Analysis & Design of a Frequency-Hopped Spread-Spectrum Transceiver for Wireless Personal Communications

Final Report

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January 1996

Funded by the US Advanced Research Projects Agency and an Industrial Consortium, with supplementary funds from the State of California MICRO Program
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ABSTRACT OF THE DISSERTATION

Analysis and Design of A Frequency-Hopped Spread Spectrum Transceiver for Wireless Personal Communications

by

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Doctor of Philosophy in Electrical Engineering
University of California, Los Angeles, 1995
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Personal Communications Services (PCS) require low-power radio technologies. One such transceiver architecture employing frequency-hopped spread spectrum techniques is described. Low power and robustness are two keys to a wireless personal communications device. A frequency-hopped code-division multiple access (CDMA) scheme is chosen over other multiple access methods because it provides an inherent immunity to multipath fading and the signal processing is performed at the hop rate, which is much lower than the chip rate encountered either in a direct-sequence CDMA or time-division multiple access (TDMA) system. This potentially results in much lower receiver power consumption. Other features such as antenna diversity with equal-gain combining and sequential hop combining are also incorporated into the transceiver design to
achieve robust wireless digital data transmission over fading channels. A direct-
conversion architecture from radio frequency (RF) to baseband reduces the overall
power consumption by eliminating intermediate frequency (IF) components. High-
rate frequency hopping with frequency-shift keying (FSK) modulation is
implemented using a direct digital frequency synthesis technique. A multiplierless
correlation FSK detector, suitable for direct-conversion receivers, has been
designed for quadrature noncoherent detection. Robust acquisition algorithms
based on energy detection and pattern matching and tracking architectures using
digital phase-locked loops are also developed for system synchronization. The
proposed transceiver is well-suited for PCS applications and other portable wireless
communications.
Chapter 1

Introduction

Recent advances in digital communications, advanced signal processing, and very-large-scale integrated circuits (VLSI) technologies have all contributed to explosive growth in personal communications. The concept of Personal Communications Services (PCS) refers to an ability for a person to communicate with another person with a PCS device anywhere without regard to location or mobility [1], [2]. Communications technology has evolved from simple wireline telephone services invented in the 19th century to advanced digital wireless communications. Although current wireline systems provide high-quality place-to-place calling capability, the pursuit of truly portable person-to-person communications, not limited by the fixed telephone equipment, still continues.

The earliest form of widespread wireless personal communications was
radio paging. It only allows one-way communication with very low data rates (typically less than 1.2 kbps). However, this technology provides the lowest power solution among the wireless communications systems currently available. It therefore offers many useful insights in the search for low-power transceiver technologies. For picocellular applications used in homes and offices, cordless phones were also developed. These have evolved into two European wireless standards (CT2 [3], DECT [4]) providing many pedestrian-based communications and telepoint services.

The first cellular system enabling mobile communications was an analog cellular system known as Advanced Mobile Phone Service (AMPS). In the past few years, second-generation cellular systems using digital communication technologies have emerged, increasing service quality and user capacity. Typical data rates are between 8-32 kbps, limiting their services to voice communications. In Europe, Global System for Mobile communications (GSM) [5], the first TDMA-based digital system, has already been in use for several years. In North America, Interim Standard 55 (IS-55), a digital TDMA standard, has increased the AMPS capacity by a factor of three by dividing an analog frequency modulation (FM) channel into three digital sub-channels. Qualcomm Inc. in San Diego, California, has also introduced the IS-95 standard [6] utilizing direct-sequence spread spectrum techniques for the commercial wireless market. The cellular systems can cover a cell radius up to one mile, requiring high transmission power (~1 W) and a
base station whose antenna is located relatively high off the ground, typically 50 meters above the ground. The existing digital wireless systems, ranging from cordless to cellular, is summarized in Appendix A.

The next generation of PCS will encompass all these existing wireless and wireline infrastructures under the umbrella of Personal Communications Network (PCN). Ubiquitous wrist-watch communications will soon be a reality with the advent of digital communication technologies for PCS, coupled with the move towards smaller microcellular wireless networks and lower RF output powers. Typical microcellular radios cover a range of a few hundred meters (about 250 meters), with a transmission power of 10 mW or less [7]. Low-power radio access technology is one of the key technical challenges for future wireless communications. The objective of this research has been to develop such a low-power, hand-held, robust communications transceiver using frequency-hopped spread spectrum (FH/SS) techniques.

In order to accomplish often conflicting design goals - low power and robustness - for a portable device, one must optimize the transceiver in all levels of the design hierarchy: system, architecture, and circuits. To achieve robustness over a multipath fading channel, system techniques such as spread spectrum and diversity combining should be incorporated into the transceiver design. The low-power requirement mandates not only the use of low-power circuit techniques such as voltage scaling and parallelism, but also the optimization of the overall hardware
architecture.

The study of these issues forms the core of this dissertation. The three principal concerns have been (1) the performance analysis of different system techniques - modulation, diversity, spread spectrum, and duplexing - by simulation; (2) wireless transceiver architecture trade-off studies and the design of digital hardware down to the logic level; and (3) the development of robust acquisition, synchronization, and tracking algorithms. The maximum data rate supported by the proposed transceiver will be 160 kbps [8], which is the standard narrowband Integrated Services Digital Network (ISDN) rate. Besides low-power PCS applications, the FH/SS transceiver can also be applicable to a wide variety commercial and military systems including microcellular phones and wireless PBX systems.

Chapter 2 deals with the system issues and the rationale behind the proposed transceiver, from the radio channel model to spread spectrum techniques. Chapter 3 is an overview of the RF and baseband transceiver architecture. Detailed baseband processing block descriptions are given in Chapter 4. Chapter 5 comments on system simulation strategies and methods used in both system performance and architecture trade-off studies. Synchronization algorithms and architectures are described in Chapter 6, followed by a summary and concluding remarks in Chapter 7. Lastly, a glossary explaining terms and acronyms is added in Appendix.
Chapter 2

System Issues

2.1 Radio Channel Model

Accurate modeling of the radio channel is crucial to understanding the impairments a radio encounters over the wireless channel and finding techniques to mitigate these effects. It also provides a basis for the system simulation model where accurate trade-off studies can be performed. Many researchers have studied indoor and outdoor radio channels, modeling the channel as a linear time-varying filter [9], [10]. Due to reflections arriving at different times, the received signal can be modeled as sum of discrete rays with different amplitudes and random phases. Turin in [11] pioneered the impulse response approach of characterizing radio channels. This model generates a conceptual channel impulse response $h(t)$, as follows:
where \( \beta_k, \tau_k, \) and \( \theta_k \) represent the magnitude, delay, and phase of the arriving paths, respectively. One way to characterize this model is by the distribution of path amplitudes. A “deep fade” occurs when these paths arrive at the receiver out of phase. During deep fades, the signal level may fall by more than 20 dB.

In a narrowband system, the significant delays \( (\tau_k) \) are confined to a small time duration relative to the symbol period. Under these conditions, (Eq. 2.1) can be approximated using the central limit theorem [12]:

\[
h (t) = Re^{j\theta}
\]  

(Eq. 2.2)

where the random variable representing the amplitude \( (R) \) is characterized by a Rayleigh distribution and the random phase variable \( (\theta) \) is uniform over \([0, 2\pi]\). The amplitude can be modeled as the joint distribution of two complex Gaussian signals, whose probability density function is given by the Rayleigh probability density [13]:

\[
Pr (r) = \frac{r}{\sigma^2} \exp\left(\frac{-r^2}{2\sigma^2}\right), \quad r \geq 0.
\]  

(Eq. 2.3)

(Eq. 2.2) represents a complex one-tap narrowband flat Rayleigh fading channel frequently encountered in the frequency-hopped radio microcellular environment where the signal bandwidth is narrow and the channel characteristics vary slowly.
Figure 2-1 shows a trajectory of these flat fading magnitudes over many hops for a variance ($\sigma^2$) of 1.

The typical path loss in a wireless multiple-access channel is modelled by the following equation:

$$P(d) = P_0 d^{-n}$$  \hspace{1cm} (Eq. 2.4)

where $P_0$ is the power received at distance ($d$) of one meter. $P_0$ depends on many factors including the transmitted power, carrier frequency, and antenna characteristics. The value of the exponent $n$ for microcellular systems is approximately 3 for outdoor channels and 4-8 for indoor channels [14]. In a radio
channel, fast Rayleigh fading (due to local multipath) is also accompanied by a slowly time-varying channel condition known as log-normal shadowing. This is mainly due to large scale reflections by mountains and tall buildings, and its average standard deviation in mean signal strength is between 6-8 dB. A typical fading track of a radio channel is shown in Figure 2-2.

![Fading Track of Multipath Radio Channel](image)

Figure 2-2 Fading Track of Multipath Radio Channel

Some important parameters that describe multipath fading channels are loosely defined below. Detailed mathematical derivations can be found in [15], [16].

- Delay spread ($\tau_m$) = the first moment of the power delay profile ($|h(t)|^2$).
- Doppler Spread ($f_d$) = $\frac{v_m}{C}$ with $v_m$ the relative motion velocity between transmitter and receiver, $C$ the velocity of radio wave propagation, and $f_c$ the carrier frequency.
- Coherence Bandwidth $\sim \frac{1}{\tau_m}$
• Coherence Time $\sim 1/f_d$

Delay spread basically denotes the range of values of the delay time over which the power delay profile $|h(t)|^2$ is significant (for example, 20 dB below the maximum power). A better measure of multipath spreading is the RMS delay spread, which is defined as the square root of the second central moment of the power delay profile $(|h(t)|^2)$. The coherence bandwidth of the channel refers to the width of the frequency band with similar channel characteristics or the bandwidth separated by two nulls in its frequency spectrum.

Typical delay spreads measured in outdoor microcellular environments are 0.5 to 1 µs. The (picocellular) indoor channel has a much smaller value, typically less than 100 ns [14]. This implies that the coherence bandwidth is as large as 10 MHz indoors and less than 1 MHz outdoors. For spread spectrum techniques to work effectively, the total spread bandwidth should be much larger than the coherence bandwidth. For our frequency-hopped system, frequency hopping sequences should be designed such that hop frequencies are separated by more than the coherent bandwidth of the channel to guarantee independent fades. The 26 MHz bandwidth available for the 900 MHz ISM band is sufficient to provide effective frequency diversity.

For a pedestrian-based microcellular system, the doppler frequency is small (about ±5 Hz for $f_c = 915$ MHz); therefore, the coherence time is much greater than the hop time. The coherence time can be interpreted as the time over
which the channel characteristics are relatively constant. It is analogous to the coherence bandwidth in the time domain. This implies that time-selective fading cannot be readily dealt with time diversity techniques, since the interleaving time may be too big. Time-selective fading and slowly varying channel conditions, however, can be abated with adaptive power control [17].

2.2 Diversity Techniques

2.2.1 Definition

Multipath fading, introduced by multiple radio-wave scatters, is the most serious impairment encountered in the radio channel, so care should be taken to lessen its effects. Diversity combining is an effective method used to deal with fading impairments. The diversity order is defined as the number of independent replicas of the transmitted signal that are processed in the receiver [15]. With \( L \)th-order diversity, the probability of error decreases with the \( L \)th power of SNR

\[
P_e = k \left[ \frac{1}{\text{SNR}} \right]^L
\]

(Eq. 2.5)

where \( k \) is a proportionality constant.

Diversity may be achieved in a combination of different domains. Spread spectrum techniques, described in detail in Section 2.4, provide frequency diversity by averaging over a wider bandwidth. Coding with interleaving (including
repeat coding over fading channels) gives time diversity. Spatial diversity can be obtained using multiple antennas coupled with different polarizations. For example, with \( L = 4 \), 30 dB of diversity gain at a BER = \( 10^{-5} \) is achieved for binary frequency-shift keying (FSK) over a Rayleigh fading channel, thereby substantially closing up the gap between the SNR required for the fading channel and that achievable in the additive white Gaussian noise (AWGN) channel (Table 2-1). In the proposed frequency-hopped transceiver, all three diversity techniques - frequency, time, and space - are incorporated into the architecture, thus resulting in a high aggregate diversity order.

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<th>BFSK</th>
<th>BPSK</th>
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<tr>
<td>AWGN</td>
<td>13 dB</td>
<td>10 dB</td>
</tr>
<tr>
<td>Rayleigh (L=1)</td>
<td>50 dB</td>
<td>45 dB</td>
</tr>
<tr>
<td>Rayleigh (L=4)</td>
<td>20 dB</td>
<td>15 dB</td>
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Table 2-1  Required SNR for BER = \( 10^{-5} \)

### 2.2.2 Diversity Combining Techniques

The issue of antenna diversity combining techniques poses an interesting question. For a handheld device operating at the 900 MHz RF range, the physical dimensions are limited, and two antennas can be separated by no more than approximately one quarter of the radio wavelength. However, it has been reported that this separation is sufficient to provide antenna diversity when the two antennas
have opposite polarizations [18].

There are three common types of antenna diversity combining techniques: maximal-ratio combining, equal-gain combining, and maximum-selection combining [13]. Maximal-ratio combining refers to combining received signal energy at different branches with their corresponding channel estimates of $R_k$ and $\theta_k$. For square-law noncoherent detection, only the Rayleigh magnitude ($R_k$) is important. In a frequency-hopped system with a high hop rate, however, maximal-ratio combining is not a viable option since it is not possible to estimate the channel state information (CSI) accurately in the short hop duration. Even with a longer averaging time, the estimated channel weights are still not useful since the fading characteristics change too fast (every hop duration).

Both equal-gain and maximum-selection combining techniques are potential alternatives. Selection between two antennas at RF is possible for a TDMA system with preambles that require only one receive branch. For an FH system where the RF carrier frequency hops over the whole band in one frame duration, both equal-gain and maximum-selection diversity techniques require signal energy combining or selection at baseband. Consequently, both schemes require two separate receive branches.

However, the performance of equal-gain combining is better than that of maximum-selection combining. The bit error rate (BER) equations of binary FSK
over the Rayleigh fading channel for equal-gain combining [15] and maximum 
signal-to-noise (SNR) selection combining [19] are shown in (Eq. 2.6) and (Eq. 
2.7), respectively:

\[
P_2(L) = \left( \frac{1}{1 + \bar{\gamma}_c} \right)^L \sum_{k=0}^{L-1} \left( \frac{1 + \bar{\gamma}_c}{2 + \bar{\gamma}_c} \right)^k
\]  
(Eq. 2.6)

\[
P_2(L) = L \sum_{k=0}^{L-1} \left( \frac{L-1}{k} \right) \frac{(-1)^k}{\bar{\gamma}_c + 2(1+k)}
\]  
(Eq. 2.7)

where \( L \) is the diversity order and \( \bar{\gamma}_c \) is the average SNR per channel, which is related to the average SNR per bit by the expression \( \bar{\gamma}_b = L \bar{\gamma}_c \). Figure 2-3 shows that the equal-gain combining scheme has a 0.5 dB SNR (in \( E_b/N_0 \)) gain when \( L = 2 \) and a 2 dB gain when \( L = 4 \) over the maximum-selection combining technique.

In practice, the selection combining receiver is implemented by selecting the receiver branch with the maximum power output (signal plus noise) at the square-law detector, since it is difficult to measure SNR. The error probability of this scheme is even worse than that of the SNR selection scheme [19]. Thus, a dual receive antenna architecture with equal-gain diversity combining was chosen as the baseline diversity combining scheme.

### 2.3 Multiple Access Schemes

Multiple access schemes share spectrum using orthogonal decomposition in the frequency, time, or code domain (Figure 2-4). There are three multiple
access schemes being used in current wireless systems. In frequency-division multiple access (FDMA), the frequency spectrum is divided and shared among different users. It can be used with both analog and digital transmission systems. For example, FDMA is used in AMPS, an analog cellular system. With the advent of digital techniques, time-division multiple access (TDMA) became feasible. In this technique, time is divided into slots which are grouped into frames. After a unique time slot in the frame is assigned through the control slots, the digital transmitter of a subscriber bursts out its data at a rate much higher than the average transmis-

Figure 2-3  Equal-Gain vs. Selection Combining

(BFSK, Rayleigh Channel)
sion rate. This intermittent behavior is the reason why TDMA is only suitable for digital transmission. Both TDMA and FDMA are band-limited since the spectrum is divided into either time or frequency slots. The third scheme, called code-division multiple access (CDMA), provides multiple access using unique code sequences. It utilizes spread spectrum techniques to share the available spectrum.

Two fundamental problems for the cellular radio channel are multipath fading and interference from other users in the cellular reuse environment. Spread spectrum techniques are effective in abating multipath because their spread bandwidth introduces frequency diversity. They are also useful in combating multi-user
interference due to their spreading using orthogonal code sequences.

There are two CDMA techniques that are used in multiple access schemes: direct sequence (DS) and frequency hopping (FH). DS-CDMA, adopted in the IS-95 cellular standard, is not band-limited but only interference-limited since every user occupies the same spectrum with different pseudo-random noise (PN) codes. Another advantage of CDMA in a multi-cell and multi-user environment is its universal frequency reuse capability. For non-DS-CDMA systems, frequencies assigned in a given cell are not used in neighboring cells to ensure sufficient spatial isolation. For example, in AMPS, a frequency reuse factor of 1/7 (one-in-seven) is employed to prevent excessive co-channel interference from adjacent cells. In DS-CDMA, the entire allocated frequency band can be shared and reused by every cell, thus increasing the overall system capacity [20].

FH-CDMA is a hybrid access technique that combines both TDMA and FDMA. Each user is assigned a set of frequencies and hops to a known frequency at every hop transition. It should be noted from Figure 2-4 that for the same transmitted power the power density of the FH signal is much higher than that of the spread DS signal, since the DS system has a much wider transmission bandwidth. In a synchronous FH-CDMA system, hopping sequences are orthogonal within the cells. In theory, there should be no intracell interference for such a system. The possibility of a one-cell frequency reuse still exists. The degradation due to intercell interference, of course, must be minimized with the help of a sufficient degree
of error correction coding, combined with interleaving. This form of access also reduces interference by assigning well-designed hopping sequences that minimize the probability of a user experiencing intercell collisions in too many frequency slots [21], [22].

One drawback of DS-CDMA, however, is a phenomenon known as the “near-far problem.” A portable close to the base station provides more power than other users far away, thus becoming a source of strong interference. Thus, adaptive power control over a wide dynamic range (about 80 dB) is essential part of the DS-CDMA system [23]. FH-CDMA systems also require a power control scheme. Although the near-far problem might not be as severe as in DS-CDMA systems, spectrum leakage from adjacent channels can be easily a problem without proper power control. FH-CDMA is chosen as the baseline access scheme for our low-power handset systems. The rationale behind this choice is discussed in the next section.

2.4 Spread Spectrum Techniques

2.4.1 Overview

Spread spectrum techniques have long been used for secure military communications, primarily because spreading mitigates the effect of intentional interference, also known as jamming. They also provide for the low probability of
intercept. In recent years, however, these techniques have been applied to terrestrial digital cellular networks, owing to their inherent immunity to multipath interference and multiple access capability. Properties of spread spectrum systems include the following [24]:

- appear “random” to an untrained observer;
- spreading digitally controlled by simple finite state machines;
- controlling mechanisms are independent of the message or data; and
- occupy a space whose dimensionality is larger than the minimum required to transmit the information in a coordinated fashion.

As a counter-example, analog frequency modulation (FM) is not a spread spectrum system because the spread signals are data-dependent.

### 2.4.2 Frequency Hopping versus Direct Sequence

A DS system spreads a narrow-band signal into a wider spectrum using a PN code. The spread signal looks essentially like noise to observers who have no knowledge of the code sequence. On the other hand, the receiver with the correct PN code can recover the original signal and discriminate other co-channel interference or jamming signals. The simplified block diagram of a DS system is shown in Figure 2-5.

For an FH system, the total available spectrum (of bandwidth of $W_{ss}$) is subdivided into a large number of frequency slots. Hop frequencies are changed at
Discrete (hop) time intervals to produce a signal that covers a much wider bandwidth. If the hop rate is greater than the symbol rate, it is called fast frequency hopping (FFH). For each symbol of information, the modulator transmits multiple copies at different frequencies. A slow frequency hopping (SFH) system is one in which the hop rate is equal to or less than the symbol rate [25]. In this case, interleaving over multiple hops can provide fade independence between contiguos symbols after deinterleaving at the receiver.
It should be noted, though, that SFH does not necessarily mean a low hop rate (LHR). It is a term defined only with respect to the symbol rate. When the symbol rate is relatively high, a SFH system can still require a high hop rate (HHR). For example, a TDMA system which hops to a new frequency every frame (e.g. hop rate \( \approx 50 \text{ Hz} \)) is also called SFH. But there are many fundamental differences in the transceiver design and implementation between a very low hop rate SFH-TDMA system and our SFH-CDMA transceiver, which hops every eight symbols. A primary difference, for example, is the need for a fast hopping synthesizer in a high hop rate system.

### 2.4.3 Processing Gain

An important characteristic of a spread spectrum system is the processing gain (PG). It is defined as the ratio of the spread bandwidth \( W_{ss} \) to the bandwidth of the information \( R_s \), which can be written in dB for a DS system as follows:

\[
P G = 10 \cdot \log \left( \frac{T_s}{T_c} \right)
\]

(Eq. 2.8)

where \( T_s \) is the symbol period and \( T_c \) is the chip period of the code. For a DS system, the co-channel interference or jamming signal is reduced by the PG, since PN code sequences are designed to be uncorrected with one another. This system can, therefore, resist multi-user interference better with a higher PG. This implies that PG directly affects the total system capacity in a DS system [26].
For an FH system, the PG is defined as follows:

\[ \text{PG} = \frac{W_{ss}}{R_s} \]  

(Eq. 2.9)

It is merely used to measure the jammer rejection gain, which is important in anti-jammer applications.

### 2.4.4 An Assessment for Low-Power Radios

The key advantages of the DS technique applied to digital cellular systems, such as universal one-cell frequency reuse, soft handoff, voice activity utilization, and no need for frequency planning, are well-documented in recent papers [20], [23], [27]. However, FH also provides some unique advantages, especially for PCS radios where low power and robustness are two key elements. Frequency selective fading effects can be reduced by spreading the narrowband signal over a band much wider the coherence bandwidth. In a DS-CDMA system, this requires a broadband radio (bandwidth > 10 MHz for indoor). For an FH system (especially for slow FH), however, the signal spectrum behaves like a narrowband system at each hop, as shown in Figure 2-4. The signal processing is performed at the hop rate, which is much lower than the chip rate encountered either in a DS-CDMA or TDMA system. This potentially results in much lower portable power consumption.

Furthermore, the synchronization requirements in an FH system are not as stringent as in a DS system. In a DS system, timing and synchronization must be
established to within a fraction of the chip interval ($T_c$). This is difficult to achieve since $T_c$ is at least an order of magnitude smaller than the hop duration as in an FH system. Therefore, an FH signal is preferred over a DS spread signal for synchronization. FH systems also have the advantage of resisting multipath fading by sending signals at different frequencies. Due to redundancy, if some of these are corrupted by interference or fading, the receiver is still able to recover the correct information by using a (sequential) hop combining receiver. Another advantage of the FH technique is frequency agility. Unlike DS, the spectrum for FH needs not be continuous or adjacent. This implies that when a narrowband interferer or jammer exists, its effect can be nullified by avoiding hopping into that frequency range. These are some of the key reasons that FH-CDMA was chosen as the multiple access scheme for our low-power handheld radios.

To date, virtually all FH systems proposed for commercial wireless applications are limited to SFH with a low hop rate, where the hopping synthesizer changes its carrier frequency slowly, once every frame or so. The FH wireless LAN at 2.4 GHz and GSM standards are two examples of such SFH systems with a low hop rate. Our system, though it is SFH by definition, still requires a high hop rate. This mandates the implementation of a fast hopping synthesizer. However, fast hopping typically requires noncoherent (NC) square-law detection because the receiver loses phase continuity whenever it hops to a new frequency. This implies
a significant SNR versus BER performance penalty. For example, NC frequency-shift keying (FSK) suffers a 6 dB SNR loss at a BER of $10^{-3}$ compared to coherent phase-shift keying (PSK), which is employed in a DS system. However, the combination of frequency diversity, minimal cochannel interference, reduced hardware complexity, and low power dissipation compared to coherent DS-CDMA systems partially compensates for this penalty and thus justifies this choice for low-power handheld devices.

2.5 Duplexing Schemes

Radio links operate in one of two modes: simplex or duplex. In the simplex mode, transmitted signals are sent over the medium in one direction only at a given time, as in walkie-talkies. A duplex scheme can be divided into two categories: full-duplex and half-duplex [28]. A full-duplex system allows simultaneous communications over the channel in both directions. In the half-duplex mode, bidirectional communication is alternated in time. The full-duplex mode is typically accomplished by frequency-division duplexing (FDD), while the half-duplex mode is achieved by time-division duplexing (TDD). Figure 2-6 illustrates duplexing techniques for a fixed carrier system. The widths of the frequency bands and time slots are artificially scaled for illustration purposes.

Although there is not much difference as seen by end-users, the proper choice of duplexing scheme impacts both the system design and the radio imple-
mentation. FDD employs two bands of spectrum separated by a certain minimum guard band, while TDD typically requires only one band. In order to achieve the same data rate to an end-user, a TDD system requires a symbol rate twice that of an FDD system. This becomes an important design consideration, especially when the transmission rate is limited by the delay spread of the RF channel. Since TDD uses the same band for both uplink (base station to portable) and downlink (portable to base station), channel reciprocity is preserved. Therefore, TDD systems can benefit when power control and antenna selection diversity schemes are employed.

To allow simultaneous bidirectional communication, an FDD system requires two separate local oscillators, one for the transmitter and the other for the receiver. In a TDD system, one local oscillator can be time-shared between transmit and receive frames. An expensive (in cost and size) frequency duplexer is also required in an FDD system which uses the same antenna for bidirectional transmission. The duplexer may also add, for example, about 2 dB of noise figure to the
RF front-end. TDD, however, does not require a duplexer. A simple RF switch or equivalent isolates transmit and receive signals from each other in time. For miniaturized PCS portables, size is often a limiting factor making TDD favorable. In addition, TDD is essential to avoid self-interference seen by the antenna when both uplink and downlink share the same band, as in DECT and our frequency-hopped CDMA system. Therefore, TDD was chosen as our baseline duplexing scheme.

2.6 Modulation Techniques

2.6.1 Trade-offs

The modulation technique chosen for the FH transceiver should allow non-coherent detection capability and constant-envelope signalling, the latter because it allows power-efficient Class-C power amplifiers. Possible candidates include non-coherent frequency-shift keying (NC-FSK) and differential phase-shift keying (DPSK). Multi-level amplitude modulation schemes such as quadrature amplitude modulation (QAM) are not frequently used in wireless systems because of severe channel degradations. Without baseband shaping filters, DPSK is not suitable for the multi-user applications since out-of-band spectral leakage corrupts signals in adjacent channels. When shaping filters are used, however, this modulation is no longer constant-envelope. Even with the use of a linear power amplifier, this modulation scheme is limited only to low hop rate systems such as SFH-TDMA where
the radio hops to a new frequency every frame. Because the first bit of each hop is
reserved to provide a phase reference to the following bits (Figure 2-7), too much
bandwidth is wasted in a high hop rate system where phase continuity between
hops is not guaranteed.

Continuous-phase modulations (CPM) such as minimum-shift keying
(MSK) and Gaussian MSK (GMSK) [29] could also be considered. These are a
class of jointly power- and bandwidth-efficient digital modulation schemes with
constant envelope which are used in IS-54 (π/4-DQPSK) and in GSM (GMSK).
The transmitted information is contained in the phase of the CPM signal:

\[
s(t) = \sqrt{\frac{2E_s}{T}} \cos \left[ 2\pi f_c t + \phi(t, \alpha) \right] \quad \text{(Eq. 2.10)}
\]

\[
\phi(t, \alpha) = 2\pi h \sum_k \alpha_i q(t - kT) \quad \text{(Eq. 2.11)}
\]

\[
q(t) = \int_{-\infty}^{t} g(\tau) d\tau \quad \text{(Eq. 2.12)}
\]

where \(E_s\) is the symbol energy, \(h\) is the modulation index, \(\alpha_i\) are the transmitted data
bits, and \( g(t) \) is the shaping pulse usually defined in instantaneous frequency as a lowpass filter. This lowpass filter, placed before the frequency synthesizer, shapes the binary input frequency to further reduce out-of-band spectral sidelobes.

When \( g(t) \) is Gaussian, it is called GMSK. MSK \((h = 0.5)\) does not require any filtering as long as the phase continuity is guaranteed. Since these signals are a form of FSK, they can be noncoherently detected by a limiter-discriminator (Figure 2-8). The performance of noncoherent detection of these signals, though, is worse than that of optimal noncoherent FSK. A penalty of 1-2 dB at a BER of \(10^{-3}\) is typically paid compared to noncoherent FSK demodulation [30]. Furthermore, clock recovery would be impossible for a high hop rate FH system due to the phase jump in each hop. These schemes are therefore ill-suited for our FH system.

![Figure 2-8 Noncoherent CPM Transceiver](image-url)
Noncoherent FSK modulation is quite suitable for an FH system. Actually, FH can be thought of as an extension of FSK where tone frequencies are not fixed. An FSK radio with FH transmits an RF frequency which is a combination of a tone frequency, a hop frequency, and a fixed carrier frequency:

\[ F_{rf} = F_{carrier} + F_{hop} + F_{tone}. \]  

(Eq. 2.13)

The hop and tone frequencies can be easily generated using a direct digital frequency synthesizer (DDFS), while the fixed carrier frequency can be produced by a voltage controlled oscillator within a phase-locked loop. Although FSK signals leak spectral energy into neighboring bins, orthogonality between frequency tones lessens the leakage problem.

### 2.6.2 Quaternary versus Binary FSK

For the proposed architecture, both binary and quaternary FSK signalling schemes are possible. For the ideal single user case, both signals have the same bandwidth efficiency, 0.5 bps/Hz. The bandwidth efficiency is defined as the ratio of the data rate \( R \) in bits per second (bps) to the bandwidth (in Hz) occupied by each user \( R_u \). For quaternary FSK, \( R \) is twice the symbol rate \( R_s \); however, it also requires twice more bandwidth compared to binary FSK. Thus, the overall ratio remains the same. The bandwidth efficiency \( B_e \) for noncoherent M-ary FSK is given by:

\[ B_e = \left( \log_2 M \right) / M. \]  

(Eq. 2.14)
For $M > 4$, the efficiency is less than 0.5, and as $M$ increases, its value goes to 0.

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Single User Case</th>
<th>Multi-User Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary FSK</td>
<td>0.5 bps/Hz</td>
<td>0.25 bps/Hz</td>
</tr>
<tr>
<td>Quaternary FSK</td>
<td>0.5 bps/Hz</td>
<td>0.33 bps/Hz</td>
</tr>
</tbody>
</table>

Table 2-2  FSK Bandwidth Efficiency

For actual multi-user scenarios where a guard band is required between user channels, however, this is no longer the case. Quaternary FSK has a 33% better efficiency than binary FSK since the same guard band is required for increased tone spacing (Table 2-2). The minimum tone separation for orthogonality in a frequency-hopped noncoherent FSK system is the maximum of the symbol rate ($R_s$) or the hop rate ($R_h$). Since our system is SFH ($R_s > R_h$), the minimum tone separation ($F_{tone}$) becomes the symbol rate, which is 80 kHz. According to the frequency tone assignment shown in Figure 2-9, the value of $R_u$ becomes four times $R_s$ for binary FSK and six times $R_s$ for quaternary FSK.

The binary format consists of tones from the set {+$F_{tone}$, -$F_{tone}$}, while the quaternary format contains tones from the set {-2$L_f_{tone}$, -$F_{tone}$, +$F_{tone}$, +2$L_f_{tone}$}. One complete tone spacing is placed between user channels to provide the minimum guard band. Tones near DC, however, are separated by two times the minimum tone spacing because the smallest tone must be located at $\pm F_{tone}$, not at $\pm F_{tone}/2$, for the chosen early-late phase detection scheme of the clock recovery
loop to work properly [31]. This guarantees the orthogonality property to hold over half of the symbol time ($T_s/2$).

Another measure to compare between different signalling schemes is the bit error rate (BER) versus signal-to-noise ratio (SNR) performance. In the AWGN channel, the probability of symbol error for M-ary FSK with noncoherent detection is given by [15]

$$P_M = \sum_{n=1}^{M-1} (-1)^{n+1} \left( \frac{M-1}{n} \right)^{1/n+1} \exp \left( -\frac{n k \gamma_b}{n+1} \right)$$  \hspace{1cm} (Eq. 2.15)

where $\gamma_b$ is the SNR per bit. The equivalent bit error probability can be obtained by

$$P_b = \frac{2^{k-1}}{2^k-1} P_M.$$  \hspace{1cm} (Eq. 2.16)

For binary FSK signals, this reduces to the simple form:
\[ P_2 = \frac{1}{2} \exp\left(-\gamma_b/2\right). \] (Eq. 2.17)

Quaternary FSK has roughly 3 dB of SNR gain (in \( E_b/N_o \)) over binary FSK since the effective signal bandwidth halves for the same bit rate. Even for the Rayleigh fading channel, simulation results show a 2.5 dB SNR gain at a BER = 10\(^{-3}\) (Figure 2-10).

One way to combat delay dispersion over the radio channel is also to use M-ary signalling, rather than binary formats. For a given data rate, this increases the effective symbol duration with respect to delay spread, thus reducing the overall delay spread problem. With all three comparisons favoring quaternary FSK signalling, it was thus chosen as the baseline modulation scheme.

Figure 2-10 Quaternary vs. Binary FSK
2.7 Capacity

The maximum system capacity or number of simultaneous users in an FH system can be calculated as follows:

\[ N = \frac{W_{ss}}{R_u} \]  
(Eq. 2.18)

where \( W_{ss} \) is again the total spread spectrum bandwidth and \( R_u \) refers to the required bandwidth per user. Since \( R_u \) is 480 kHz (including the guard band) for 4-ary FSK (\( R_s = 80 \) kHz), this results in about 54 possible user slots over the total 26 MHz ISM bandwidth. This satisfies the FCC specifications that require at least 50 hopping channels in the 902-928 MHz band.
Chapter 3

Transceiver Architecture

3.1 General Overview

Prime considerations for a personal handheld device are low power, portability, and robustness. Low power dissipation is required to prolong battery life. Portability implies minimal size and weight. The handset should also be designed to guarantee robust transmission over the wireless channel. The necessary signal processing functions of a frequency-hopped transceiver include the following: up/downconversion, hop/dehop, modulation/demodulation, synchronization, control, and input/output (I/O) processing (Figure 3-1).

3.1.1 Architectural Trade-offs

A system’s architecture defines the implementation of the necessary func-
tions of the given system. There are two basic types of transceiver hardware architectures: superheterodyne or direct-conversion (Figure 3-2). A superheterodyne receiver, widely used in current cellular systems, converts the RF signal to baseband through one or more intermediate frequency (IF) stages, thus providing a wide dynamic range and good selectivity for the received signal. These can be further classified as high-IF or low-IF architectures (Figure 3-3), depending on the IF frequency range relative to the baseband signal spectrum.

Direct-conversion transceivers have been gaining much attention for portable communications applications where low power and small area are key require-
ments [32]. A direct-conversion architecture, also known as a homodyne or zero-IF architecture, converts the signal from RF directly to baseband or vice versa, with no IF conversion step. This eliminates image-reject filters and other IF components, thereby making high integration possible. Thus, a direct-conversion architecture has been adopted for our transceiver.

Carrier recovery, though, is difficult for a direct-conversion receiver since it has to be done at RF. This is still the primary reason why most direct-conversion receivers use a noncoherent detection scheme where carrier recovery is not necessary. Since our FSK detection is done noncoherently, the direct-conversion architecture is well-suited for our receiver. Table 3-1 summarizes the benefits and
drawbacks of the three competing receiver architectures. It should be noted that a typical superheterodyne transceiver requires at least three types of filters - RF, image-reject, and channel-select filters. Image-reject filters are, however, eliminated for both zero-IF and low-IF architectures.

Analog and digital partitioning is another criterion used to classify transceiver architectures. With advances of digital signal processing and high-speed
analog-to-digital converter (ADC) technologies, IF-sampling receivers are replacing typical baseband sampling receivers. For coherent reception applications such as quadrature amplitude modulation (QAM), digital IF receivers provide accurate I-Q generation, allowing carrier and timing recovery to be implemented purely in the digital domain. For our transceiver, the analog and digital partitioning is performed in such a way to simplify the overall hardware architecture (refer to Section 3.2).

<table>
<thead>
<tr>
<th>Benefits</th>
<th>High-IF Architecture</th>
<th>Zero-IF Architecture</th>
<th>Low-IF Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Benefits</td>
<td>Wider dynamic range</td>
<td>High integration (one or two chip solution)</td>
<td>No DC offset problem</td>
</tr>
<tr>
<td></td>
<td>Good rx sensitivity</td>
<td>Low cost, Low power</td>
<td>High integration possible</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Easier carrier recovery</td>
</tr>
<tr>
<td>Drawbacks</td>
<td>Costly discrete filters</td>
<td>DC offset problem</td>
<td>I-Q matching critical</td>
</tr>
<tr>
<td></td>
<td>Low integration</td>
<td>Tougher RF ICs specs</td>
<td>Image signal suppression</td>
</tr>
<tr>
<td></td>
<td>High power</td>
<td>High DR circuits</td>
<td>Extra ADC dynamic range</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I-Q matching important</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Carrier recovery hard</td>
<td></td>
</tr>
<tr>
<td>Filters</td>
<td>RF, Image-reject, Channel</td>
<td>RF, Channel</td>
<td>RF, Channel</td>
</tr>
<tr>
<td>Suitable Applications</td>
<td>Systems with fixed IF</td>
<td>Noncoherent modulation with no energy at DC (NC-FSK)</td>
<td>Linear modulation with BB spectrum around DC (GMSK)</td>
</tr>
</tbody>
</table>

Table 3-1 Architecture Trade-offs Summary

3.1.2 Single-Sideband Modulation

Direct-conversion transmitters quite often utilize Weaver’s single-sideband modulation (SSB) technique [33]. When a baseband FSK signal is upconverted to
RF without using the SSB technique, it will produce both the desired tone and its image symmetric around the carrier frequency:

\[
\cos (2\pi f_c t) \cdot \cos (2\pi f_x t) = \frac{1}{2} \{ \cos [2\pi (f_c + f_x) t] + \cos [2\pi (f_c - f_x) t] \} \quad \text{(Eq.3.1)}
\]

where \( f_c \) is the fixed RF carrier frequency and \( f_x \) corresponds to the combination of the hop frequency and the tone frequency (Figure 3-4). A very narrow bandpass filter can remove the unnecessary image. However, building such a narrow bandpass filter at high frequencies is not an easy task, especially when an on-chip filter is required for monolithic integration.

Figure 3-4  Real Mixing Spectrum

The SSB technique provides an effective way to suppress the image signal without resorting to bandpass filters with sharp roll-off. The function of the SSB modulation can be mathematically explained using complex-signal representa-
The two equations above convey two important properties of SSB modulation, both of which employed in our transceiver architecture. The first is that only the desired tone is produced by taking the real part of the multiplication of two complex signals. Secondly, the choice of the sign of $f_x$, which is controlled digitally by the input frequency control word of the DDFS, determines whether the generated signal will be either upper sideband or lower sideband with respect to the carrier frequency (Figure 3-5). This suggests that a quadrature digital synthesizer which spans only

$$I_{USB} (t) = \text{Re} \{ \exp (j2\pi f_c t) \cdot \exp (j2\pi f_x t) \} = \cos [2\pi (f_c + f_x) t] \quad (\text{Eq. 3.2})$$

$$I_{LSB} (t) = \text{Re} \{ \exp (j2\pi f_c t) \cdot \exp (-j2\pi f_x t) \} = \cos [2\pi (f_c - f_x) t]. \quad (\text{Eq. 3.3})$$

![Figure 3-5  Single-Sideband Modulation Technique](image-url)
half the required band (13 MHz) can effectively achieve the total 26 MHz of hopping bandwidth using this sign technique. In fact, this is one of the key factors that were exploited to implement the low power digital hopping synthesizer [34].

3.2 Overall Architecture

The proposed frequency-hopped transceiver employing such novel architectural techniques as direct conversion, SSB modulation, hard-limiting, and quadrature demodulation is shown in Figure 3-6. The transceiver integrates all RF, IF, and baseband processing components into a monolithic solution. One of the most critical components of a frequency-hopped transceiver is a low-power hop-

![Figure 3-6 Overall FH/SS Transceiver Architecture](image-url)
Conventional hopping synthesizers use analog phase-locked loop techniques. The analog PLL-based synthesizer has programmable frequency dividers in the loop to generate different frequencies, as shown in Figure 3-7. Although it has certain advantages such as wide tuning range and good spectral purity, the fundamental problem of this analog frequency synthesizer is its speed and limited frequency resolution. The hopping speed of the analog synthesizer is limited by the settling time of the loop which is inversely proportional to the loop bandwidth. Typical settling times of these analog hopping synthesizers are on the order of few hundreds of microseconds [35].

![Figure 3-7  Analog PLL-Based Frequency Synthesizer](image)

A direct digital frequency synthesis technique [36] combined with a digital-to-analog converter (DAC) provides an alternative implementation of a fast frequency-agile synthesizer. Samples of a sine wave are generated directly from the sine ROM which is addressed by the output of a digital phase accumulator (Figure
The frequency resolution \( (F_{\text{clk}}/2^N) \) of this synthesizer is determined by its wordlength \((N)\) and the output frequency is given by

\[
F_{\text{out}} = \frac{F_{\text{clk}}}{2^N} \cdot F
\]

(Eq. 3.4)

where \(N\) is the number of bits in the phase accumulator, \(F_{\text{clk}}\) is the frequency of the system clock, and \(F\) is the value of the frequency control register.

The DDFS approach has several key advantages over conventional analog PLL-based synthesizers, the most important of which is being able to achieve rapid frequency changes with continuous phase. The hop rate is no longer limited by the RF synthesizer settling time but by the system requirements. The discrete hop frequencies are determined by a PN code sequence stored in the memory before the input control register of the DDFS. The spectral quality of a DDFS system is related to a number of factors including phase truncation, amplitude quantization, DAC linearity, and the phase noise of the clock source. The specifications

Figure 3-8  Direct Digital Frequency Synthesizer

The DDFS approach has several key advantages over conventional analog PLL-based synthesizers, the most important of which is being able to achieve rapid frequency changes with continuous phase. The hop rate is no longer limited by the RF synthesizer settling time but by the system requirements. The discrete hop frequencies are determined by a PN code sequence stored in the memory before the input control register of the DDFS. The spectral quality of a DDFS system is related to a number of factors including phase truncation, amplitude quantization, DAC linearity, and the phase noise of the clock source. The specifications

42
of the DAC, filter, and DDFS circuits are chosen such that 50 dB spectral purity can be achieved in our frequency synthesizer system.

The detailed RF architecture description is beyond the scope of this dissertation, and thus only functional descriptions of the RF architecture are mentioned here. Obviously, the SSB modulation technique requires both a quadrature DDFS and a quadrature local oscillator (LO). In-phase and quadrature carrier signals of the LO are generated using a polyphase oscillator [37]. The phase noise of the LO should be small enough so that both the in-band phase noise and the total distortion added to the received signal by the phase noise spectrum of other transmitters located nearby in frequency are at least a certain threshold below the desired signal. The out-of-band phase noise requirement gives the following criterion for the averaged phase noise spectral density \( N_o \) in dBc/Hz:

\[
N_o = -\left[ \frac{S/N \text{ Threshold} + \text{Signal BW} + \text{No. of Users}}{\text{(in dB)}} \right]. \quad (\text{Eq. 3.5})
\]

Assuming a 40 dB S/N threshold, 80 kHz signal bandwidth and total of 50 users in our system, this value becomes -106 dBc below the carrier signal at one channel spacing away, which is 480 kHz on average for the 4-ary FSK case. By using the digital frequency synthesis technique coupled with the inherent matching of monolithic CMOS analog circuits, 45 dB of SSB image rejection can be achieved without any trimming or feedback loops. Since constant-envelope FSK modulation is used and adaptive power control is required, an output programmable class-C
power amplifier [38] is implemented for transmission.

In the receiver, the dehopping and downconversion process is performed in a single direct-conversion stage to save power. Quadrature downconversion is required to efficiently use the entire 26 MHz transmission bandwidth (Figure 3-9).

If real conversion (mixing) is used, half the transmission bandwidth will be wasted in order to avoid image aliasing. Quadrature downconversion, however, requires both in-phase and quadrature branches. It would be difficult to generate accurate I-Q dehopping carriers over the entire 26 MHz band using a conventional passive phase splitter. A desirable by-product of the SSB modulation technique is that if we take the imaginary part of the complex signal (Eq. 3.6), we get a signal which is orthogonal to the original signal obtained by taking the real part (Eq. 3.2). This technique is used to generate an accurate quadrature carrier signal at RF.
Direct downconversion can be implemented using either a continuous-time or a subsampling mixer technique. A continuous-time mixer is typically implemented using a (linear) Gilbert-cell multiplier or its variations [39]. Subsampling downconversion is an interesting technique which combines both the mixing and sampling processes in one step. A subsampling mixer [40] can be thought of an ideal sampler with a sampling frequency chosen to meet the harmonic constraint and the Nyquist criterion (Figure 3-10). Thus, the mixing frequency need not be as high as the original RF carrier as long as one of its harmonics covers the RF signal spectrum. Since mixing in the time domain is equivalent to convolution in the frequency domain, the signal spectrum after subsampling becomes

\[
Q_{USB}(t) = \text{Im} \left\{ \exp(j2\pi f_c t) \cdot \exp(j2\pi f_x t) \right\} = \sin [2\pi (f_c + f_x) t] \quad \text{(Eq. 3.6)}
\]
where

\[
\frac{1}{2} \sum_n \{ F(f - f_c - nf_s) + F(f + f_c - nf_s) \} \tag{Eq. 3.7}
\]

\[
\frac{1}{2} \{ F(f - f_c) + F(f + f_c) \} \tag{Eq. 3.8}
\]

is the original RF spectrum, which is band-limited appropriately. If \(f_c = kf_s\) for an integer \(k\), this equation is simplified to:

\[
\sum_n F(f - f_s) . \tag{Eq. 3.9}
\]

This is precisely the result obtained by a continuous-time mixing by \(f_c\), followed by lowpass filtering and sampling by a clock with \(f_s\), but with much simpler hardware.

One problem with this type of mixer is, however, thermal aliasing noise due to sampling which worsens the total noise figure. Moreover, the required RF bandpass filter should now also function as an anti-aliasing filter. If a strong interference signal exists outside the band of interest, the specifications of the RF bandpass filter must be tighter in order to avoid possible signal aliasing. A subsampling architecture is best-suited for FDD systems where there are two separate synthesizers for transmit and receiver, since the receive synthesizer is independent of the transmit synthesizer. For a TDD system which shares the synthesizer between the transmit and receive branches, the original RF frequency is required for transmission. Thus, the receiver carrier has to be divided from the existing RF carrier,
which is inefficient.

### 3.2.1 System Clocking Strategy

It is desirable to reduce the number of crystal oscillator sources for the transceiver design in order to minimize harmonic coupling and other distortions possible with a multi-oscillator system. For our transceiver, only one clock reference is possible with careful frequency planning. Since our handset is a TDD system, one LO can be shared between the transmitter and receiver. Other clock

![Transceiver Clocking Scheme](image_url)

**Figure 3-11** Transceiver Clocking Scheme
frequencies are carefully chosen so that they can all be derived from the LO frequency (915 MHz). The DDFS clock frequency is chosen as 76.3 MHz, which is the LO frequency divided by 12. For the receive path, the sampling clock frequency of the switched-capacitor filter front-end (decimator) is chosen to be 57.2 MHz (the LO frequency divided by 16), followed by a 14.3 MHz (the LO frequency divided by 64) lowpass filter block. For the demodulator, the correlator front-end is sampled at 7.15 MHz, while low-rate clocks such as the symbol clock are generated from the numerically-controlled oscillator (NCO) which is also clocked at 7.15 MHz. Figure 3-11 shows the clocking strategy for the entire transceiver.

3.2.2 Implementation Imperfections

3.2.2.1 DC Offset

The direct-conversion architecture potentially suffers from a DC offset problem [32]. For a baseband signal of 300 µV in the direct-conversion receiver, for instance, the DC offset can be as high as a few mV, thus totally wiping out the received signal. Two main sources for this problem are mismatches in the baseband receive signal path and self-mixing of LO leakage which is often time-varying. Figure 3-12 shows the frequency spectrum of the DC offset with the binary FSK case for our receiver. Just as each tone has a signal bandwidth associated with it, the DC offset signal is also modulated in frequency by the offset bandwidth,
denoted here as $F_{\text{offset}}$.

Figure 3-12  DC Offset Spectrum

For a TDMA system like GSM, which has a fixed carrier frequency, the offset bandwidth is only a few hertz and is dominated by the rate that a user moves his hand with a portable. For our frequency-hopped system, though, $F_{\text{offset}}$ can be as high as the hopping rate (10 kHz) if there is a significant variation of the DC offset levels between hops. This variation is not expected to be much since the hop bandwidth is narrow with respect to the carrier frequency (~1 GHz). However, actual measurements with a prototype need to be carried out in order to accurately characterize this variation.

There are several techniques that can be to mitigate the DC offset problem. From the architectural point of view, a new type of superheterodyne receiver, called a “low-IF receiver” because its IF is close to baseband, has been proposed for some GSM handsets [41]. However, this technique requires complex image
suppression techniques which are a serious bottleneck for this solution (Figure 3-3). Since the image signal is not its own, this signal can be dominant in the presence of severe multipath fading (possibly > 20 dB higher).

A DC feedback loop either in the analog domain or in the mixed-signal domain can be used to mitigate this effect. For FSK signals, which do not have any energy at DC, simple AC coupling can also be used. Functionally, the DC feedback loop is identical with the AC coupling block. Both of them are effectively a highpass filter (HPF). The 3-dB corner frequency of the filter or the loop should be designed such that the DC offset signal is attenuated by at least 20 dB compared to the (minimal) detectable signal level. It should be noted, though, that the total attenuation comes from a combination of the HPF attenuation and the offset signal level itself. If the offset signal is relatively low, the attenuation of the filter can be relaxed. The AC coupling block has the following highpass characteristic:

\[ H(jw) = \frac{jwCR}{jwCR + 1} \text{.} \quad (\text{Eq. 3.10}) \]

The linearized model of the discrete-time DC feedback loop is shown in Figure 3-13(a). The first-order digital accumulator works as a lowpass filter \( L(z) \) by averaging over the instantaneous error signals. The loop transfer function (Eq. 3.11) also shows a highpass characteristic. The loop bandwidth is determined only

\[ H(z) = \frac{E(z)}{I(z)} = \frac{1 - z^{-1}}{1 - z^{-1} + Kz^{-1}} \text{.} \quad (\text{Eq. 3.11}) \]
by the loop constant \((K)\) and the clock rate \((F_{clk})\), as shown in Figure 3-13(b). For those systems using linear modulation techniques with significant energy at DC, the DC compensation technique is very sensitive to the loop bandwidth. Figure 3-14 shows the DC offset simulation effects over different loop bandwidths for binary PSK (BPSK) with raised-cosine filtering (50% excess bandwidth) at 150 kbps. If
the DC offset varies more rapidly than 5 Hz, this technique is no longer effective due to severe energy loss near DC.

For AC coupling, the value of the coupling capacitance cannot be very large if on-chip implementation is desired. The analog DC feedback loop has the advantage over the AC coupling block since the R-C components can be placed away from the signal path. The 3-dB corner frequency ($F_{3dB}$) can thus be controlled by external components. For this reason, we have adopted a DC feedback loop around the analog baseband components (hard-limiter). Figure 3-15 shows the effectiveness of the DC-offset compensation technique in our system. No noticeable degradation is observed until $F_{3dB}$ extends to more than a quarter of the tone frequency. This validates the suitability of FSK modulation for direct-conver-
sion receivers.

A direct-conversion transceiver requires analog I-Q carrier generation. However, I-Q mismatches, both in amplitude and phase, will degrade the hardware performance. The mismatches translate into two problems. For the transmitter, the SSB technique deviates from the ideal case, thus producing an unwanted image

\[ F_{c} - F_{x} \]

\[ F_{c} + F_{x} \]

\[ \text{Sideband Suppression Ratio} \]

\[ \text{USB} \]

\[ \text{LO Leak} \]

\[ \text{LSB} \]

\[ 10^{-1} \]

\[ 10^{-2} \]

\[ 10^{-3} \]

\[ 10^{-4} \]

\[ 4.0 \]

\[ 6.0 \]

\[ 8.0 \]

\[ 10.0 \]

\[ \text{Eb/No (dB)} \]

\[ \text{BER} \]

\[ \text{Mag (dB)} \]

\[ -50.0 \]

\[ -30.0 \]

\[ -10.0 \]

\[ \text{Freq (Hz)} \]

\[ 3t \]

\[ 5t \]

\[ 7t \]

\[ -7t \]

\[ -5t \]

\[ -3t \]

\[ -t \]

\[ t \]

\[ 3t \]

\[ 5t \]

\[ 7t \]

\[ (a) \text{ BER vs. SNR (AWGN)} \]

\[ (c) \text{ Spectrum} \]

\[ (b) \text{ LO Leak} \]

\[ (d) \text{ Sideband Suppression Ratio} \]

\[ (e) \text{ USB} \]

\[ (f) \text{ LO Leak} \]

\[ (g) \text{ LSB} \]

\[ (h) \text{ Fc - Fx} \]

\[ (i) \text{ Fc + Fx} \]

\[ (j) \text{ Fc} \]

\[ (k) \text{ Spectrogram} \]

\[ (l) \text{ Single-Sideband Modulation Imperfections} \]

\[ (m) \text{ Ideal} \]

\[ (n) \text{ Fc} \]

\[ (o) \text{ Fc - 10kHz} \]

\[ (p) \text{ Fc - 20kHz} \]

\[ (q) \text{ Fc - 25kHz} \]

\[ (r) \text{ BER vs. SNR (AWGN)} \]

\[ (s) \text{ Spectrum} \]

\[ (t) \text{ Sideband Suppression Ratio} \]

\[ (u) \text{ USB} \]

\[ (v) \text{ LO Leak} \]

\[ (w) \text{ LSB} \]

\[ (x) \text{ Fc - Fx} \]

\[ (y) \text{ Fc + Fx} \]

\[ (z) \text{ Fc} \]

\[ \text{Figure 3-15} \text{ DC Offset Compensation for 4-FSK} \]

\[ \text{3.2.2.2 I-Q Mismatches} \]

A direct-conversion transceiver requires analog I-Q carrier generation. However, I-Q mismatches, both in amplitude and phase, will degrade the hardware performance. The mismatches translate into two problems. For the transmitter, the SSB technique deviates from the ideal case, thus producing an unwanted image

\[ \text{Ideal} \]

\[ F_{c} - 10kHz \]

\[ F_{c} - 20kHz \]

\[ F_{c} - 25kHz \]

\[ \text{BER} \]

\[ \text{Eb/No (dB)} \]

\[ 10^{-5} \]

\[ 10^{-4} \]

\[ 10^{-3} \]

\[ 10^{-2} \]

\[ 10^{-1} \]

\[ 10^{0} \]

\[ 10^{1} \]

\[ 10^{2} \]

\[ 10^{3} \]

\[ 10^{4} \]

\[ 10^{5} \]

\[ \text{SNR (AWGN)} \]

\[ \text{Ferrittin 118} \]

\[ \text{Figure 3-16} \text{ Single-Sideband Modulation Imperfections} \]

\[ \text{Figure 3-17} \text{ SSB Technique Deviation} \]
signal (Figure 3-16). The effect of degradation is captured in the following equation [42]:

\[
\frac{P_{spur}}{P_{desired}} = \frac{1 + \gamma^2 - 2\gamma \cos \phi}{1 + \gamma^2 + 2\gamma \cos \phi}
\]  
(Eq. 3.12)

where \(\gamma\) is the gain ratio of the I-Q branches (\(I/Q\)) and \(\phi\) is the phase error (the deviation from \(\pi/2\)). For instance, with a 3 degree phase mismatch and a 3% amplitude deviation, the maximum achievable SSB suppression is only 35 dB. For the receiver, the I-Q mismatches affect the orthogonality property of I-Q signal pairs. A monolithic design with careful transistor matching, though, can guarantee reasonable I-Q matches: typically, a phase mismatch of 1 degree and a gain imbalance of 2%. If further accuracy is required, the designer must resort to other advanced techniques such as device trimming and some type of gain and feedback

![Figure 3-17  I-Q Mismatch Simulation](image-url)
loop.

The combined effects of I-Q mismatches have been simulated for our transceiver (Figure 3-17). The unwanted SSB image of a transmitter is modeled as a co-channel interference to another user. Simulation results have shown that there

![Figure 3-18 Performance Sensitivity to Mismatches](image)
is little degradation, as long as the SSB image is suppressed more than 35 dB below the desired signal. The issue of sensitivity to mismatches was also studied via simulation (Figure 3-18). The received signal is relatively insensitive to mismatches: the amplitude mismatch is unimportant due to hard-limiting, and the phase mismatch is less critical since the orthogonal FSK signals are detected non-coherently. Since our system is more sensitive to the transmitter I-Q mismatches than the receiver mismatches, the more strict requirement of a 45 dB SSB image suppression is specified for the transmitter.

### 3.3 Baseband Architecture

Low power dissipation requires that complex signal processing such as adaptive equalization and carrier recovery be avoided if possible. Delay spread ($\tau_m$) without countermeasures (equalization) determines the upper limit of the transmission rate through the radio channel. For outdoor microcellular channels, the delay spread value is around 0.5 $\mu$s. This implies that there will be about 0.5 $\mu$s of delay dispersion due to group delay variations over different carrier frequencies. For a fast frequency-hopped system, this delay cannot be tracked by the time recovery loop. The delay spread should therefore be a fraction of the baud time, typically one tenth or less [43]. This suggests that the maximum transmission symbol rate possible without resorting to an expensive wideband channel equalizer is about 100 kHz. Our modulation baud rate (80 kHz) was appropriately chosen for
this requirement. Thus, no equalization is required for our receiver.

3.3.1 Baseband Transmitter

The baseband transmitter, shown in Figure 3-19, is quite simple for our system, since both FSK and FH are achieved using the DDFS. Only two other blocks are required besides the DDFS/DAC combination: an encoder that translates the input symbol into an appropriate quaternary FSK frequency and a memory that stores the frequencies which correspond to the hopping patterns. These two frequencies are summed at every baud cycle and fed into the frequency control word of the DDFS for proper tone generation. A signal invert option is added into the modulator to control the possible spectral inversion at the receiver. The use of the DDFS results in continuous phase changes between different frequencies which makes the transmitted FSK signal a form of continuous-phase modulation (CPM). Note in Figure 3-20 that the sidelobes of continuous-phase FSK (CPFSK)
are lowered to 27 dB below the peak, compared to only 13 dB for the non-CPFSK case. Although the phase continuity of the CPM process cannot be utilized at the receiver since the channel introduces a phase jump between hops, low spectral sidelobes of the transmitter CPM spectra are still beneficial for multi-user radio scenarios.

![Figure 3-20 Power Density Spectra of FSK](image)

**3.3.2 Baseband Receiver**

Automatic gain control (AGC) is required if the dynamic range of the
detector is less than that encountered in the radio channel (typically 60-80 dB). A conventional AGC loop architecture is shown in Figure 3-21. The medium-term variations of the channel such as shadowing are handled by the AGC loop, while the long-term variations such as path loss and time-selective fading (tunneling) are accommodated by adaptive power control. Typically, a few extra bits (3-4 bits) of resolution are required on the ADC to handle short-term multi-path fading.

![Conventional AGC Loop Architecture](image)

Figure 3-21 Conventional AGC Loop Architecture

Since FSK signalling only involves the frequency information, not amplitude or phase, a hard-limiter capable of more than 80 dB of dynamic range replaces an actual AGC loop. The hard-limiter works as a one-bit quantizer and makes the received signal independent of level variations. Before hard-limiting, of course, a lowpass channel filter selects the baseband signal from neighboring channels. The filter should have a wide dynamic range. Basically, a direct-conversion receiver of this nature requires that all of the building blocks, including baseband components, have a high enough dynamic range to avoid any gain control (Figure
The RF-to-baseband gain \((G)\) should be distributed appropriately among the analog components in such a way to minimize the total noise level. The minimum detectable level of the system is determined by the receiver sensitivity, while the maximum level of the dynamic range is limited by the linearity of the RF front-end.

The receiver sensitivity is defined in decibels as [44]

\[
Rx \text{ Sensitivity} = -174 \, dBm + NF + Noise \, BW + SNR \quad (Eq. \, 3.13)
\]

where \(-174 \, dBm\) represents the thermal noise \((kT)\) in a 1-Hz bandwidth at 300 K and \(NF\) denotes noise figure of the receiver. With 7 dB of total noise figure (including the antenna and bandpass filter loss), 80 kHz of noise bandwidth, and 10
dB of SNR threshold (AWGN), the receiver sensitivity for our system is -108 dBm. An extra 20 dB should be added to this value if the worst-case Rayleigh fading channel is considered. The hard-limiter mated with the digital FSK detector was evaluated for dynamic range. The measured dynamic range of the detector is 82 dB at a BER of $10^{-3}$ [45], which is sufficient for the radio channels encountered in most wireless applications. The minimum detectable signal power at a BER of $10^{-3}$ was measured to be -72 dBm, which is mostly dominated by the input noise of the limiting amplifier. The upper limit, however, is set by the maximum output swing of the stage driving the limiter, which is 1 V peak-to-peak for the test case. For the FSK detector alone, there is no inherent upper limit and the limiter input may swing to the power supply levels.

Due to odd harmonics produced by hard-limiting the sine waves, our approach limits the modulation scheme to binary FSK for real signal detection and to quaternary FSK for complex signal detection (Figure 3-23). However, the merits from power savings and hardware simplicity obtained from the absence of a multi-bit analog-to-digital converter (ADC) and an expensive (in both power and complexity) linear variable gain amplifier required in the AGC loop justify this architecture for a portable transceiver design.

This receiver architecture results in an all-digital quadrature FSK demodulator using an oversampled one-bit correlation detection scheme. This demodulator, unlike Fast Fourier Transform (FFT) or matched filter methods, provides a
flexible design which can easily accommodate programmable data rates. The same hardware can also be used to demodulate both data and synchronization hops. To guarantee robust digital data transmission, the receiver also incorporates dual antenna diversity. Consequently, the demodulator needs to combine the FSK tone energies of the two receiver branches.

The worst-case accuracy of a crystal oscillator without complicated compensation techniques is typically ±50 ppm (parts per million). With open-loop direct conversion from a 915 MHz RF to baseband, the carrier frequency error could deviate up to ±100 kHz (including the transmitter error as well). The receiver therefore requires a frequency tracking loop, not for phase tracking of the carrier as in a coherent receiver, but for compensating for the frequency offset between the
transmitter and receiver. A baud tracking loop is also required to recover the clock from the received data. Both loops use a digital phase-locked loop (PLL) architecture with programmable loop coefficients.

Since our system is slow frequency-hopped, the hop rate is lower than the symbol rate, thus allowing the use of an open-loop hop time synchronization scheme in which the hop time is aligned with the symbol time plus a programmable delay to compensate for the delay between the two loops. The delay should account for the average group delay of the lowpass filter plus the pipeline delay of the DDFS/DAC combination. It is mostly dominated by the filter group delay (~3 \( \mu \text{s} \)); however, the actual value should be measured during testing and pro-

![Baseband Receiver Block Diagram](image)

**Figure 3-24** Baseband Receiver Block Diagram
grammed accordingly. Figure 3-24 shows the proposed baseband receiver block
diagram, containing a diversity-combining FSK demodulator, and time and fre-
quency tracking loops. The following sections contain the detailed descriptions of
the channel-select filter and the FSK detector.

3.3.2.1 Channel-Select Filter

A. Specifications

For a direct-conversion receiver, channel selection is performed at base-
band using a lowpass filter. Given the quaternary frequency tone assignment
described in Section 2.6.2, the channel-select filter specifications are summarized
in Table 3-2. The stopband frequency actually corresponds to a tone from the adja-
cent user; therefore, a minimum of 50 dB rejection is required. It then guarantees
24 dB of rejection at the 6-dB signal bandwidth of the unwanted tone. Notice in
Figure 2-9 that the 6-dB signal bandwidth for a quaternary tone at a baud rate of 80
kHz extends to ±40 kHz around the tone frequency.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passband Edge</td>
<td>230 kHz</td>
</tr>
<tr>
<td>Stopband Edge</td>
<td>320 kHz</td>
</tr>
<tr>
<td>Passband Ripple</td>
<td>&lt; 1 dB</td>
</tr>
<tr>
<td>Stopband Attenuation</td>
<td>&gt; 50 dB</td>
</tr>
</tbody>
</table>

Table 3-2 Channel-Select Filter Specifications

The noise bandwidth of the entire analog system is set by the passband of
the channel-select filter (230 kHz). The passband frequency is chosen such that there is no significant energy loss for desired signals, and the group delay whose peak occurs at the corner frequency is relatively small over the frequency of interest. The latter condition limits the variation of the group delay over the signal bandwidth. The sharp transition of this channel filter requires a relatively high-Q design. Therefore, a sixth-order elliptic filter is required. Other IIR filter structures require an even higher order, as listed in Table 3-3. An FIR filter is not an option since its order is too high for practical consideration.

<table>
<thead>
<tr>
<th>Type</th>
<th>Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elliptic</td>
<td>6</td>
</tr>
<tr>
<td>Chebyshev</td>
<td>9</td>
</tr>
<tr>
<td>Butterworth</td>
<td>20</td>
</tr>
<tr>
<td>FIR (Equiripple)</td>
<td>133</td>
</tr>
</tbody>
</table>

Table 3-3 Channel-Select Filter Order Estimation

The group delay over the signal bandwidth is not constant (Figure 3-25). However, for our FSK detector, this is not a limiting factor. The main distortion comes from the filter’s transient effects, not from the group delay variations. Thus, an IIR elliptic filter structure is acceptable. The channel-select filter is implemented using a switched-capacitor (SC) technique for its precise tuning capability [46]. The high selectivity requirement of the filter makes a continuous-time implementation almost impractical without a tuning circuit in a feedback loop. When
programmable bandwidths and data rates are required, the SC filter also has a distinct advantage over the continuous-time filter since its bandwidths scale with the
sampling clock rate. Though a ladder structure implementation has the least sensitivity to the filter coefficient variations, a biquad implementation with a gain between stages can achieve a higher dynamic range by reducing the input noise of the filter. Since our direct-conversion receiver mandates that all components have a wide dynamic range, a sixth-order SC filter using a biquad structure was chosen for the channel filter implementation.

B. Filter Distortion

When an FSK signal passes through a band-limiting filter, the signal gets distorted both in amplitude and zero-crossing locations. When this happens at baseband with a highly selective lowpass filter, the distortion becomes even worse since there are only one or two cycles per baud. There are two main sources for transient filter distortions. First, the lowpass filter distorts the signals at data transitions, as shown in Figure 3-26(a), since there are 180 degree phase changes when data is alternating between 1 and 0. This is inherent in any direct-conversion receiver using a complex signalling scheme because of unavoidable phase jumps between positive and negative frequencies. Alternate demodulation schemes have been examined to alleviate this problem. First, half-cycle demodulation, in which only half of the signal samples in the middle are used for detection, was investigated. This approach can reduce the filter distortion by ignoring the samples at the transition boundaries. However, this results in inherent SNR loss, since the signal
power is reduced by half; thus, it is not useful. Real demodulation, instead of quadrature demodulation, also has a potential to minimize the distortion, since it guarantees continuous phase between symbols within each hop. This scheme, though, suffers from capacity loss, since half of the spectrum will be wasted in order to avoid signal aliasing. Thus, it is not utilized.

For a frequency-hopped system, phase discontinuity is also experienced at hop boundaries as shown in Figure 3-26(b). An FH system should guarantee independent fades in each hop, which is required for diversity combining and channel decoding. For a fast FH system, this is achieved by hopping many different frequencies for each symbol; however, the transient filter distortion problem becomes worse by doing so. Slow FH with interleaving alleviates this problem while maintaining independent fading between symbols when properly deinterleaved at the receiver (mainly because phase jumps between hops occur much less frequently). The operation of slow FH with interleaving is pictorially explained in Figure 3-27.
for a 4x4 block interleaving case.

Simulation results have shown that slow FH significantly reduces the overall channel filter distortion effects (Figure 3-28). In order to balance the perfor-

![Figure 3-27 Slow FH with Interleaving (4x4 Block Interleaving)](image)

![Figure 3-28 Hop Rate Simulation](image)
mance improvement with the interleaver complexity and processing delay penalty, a rate of 8 symbols per hop was chosen as the baseline hop rate. The detailed description of the proposed interleaver/deinterleaver block is given in Chapter 4.

3.3.2.2 FSK Detector

A. Backgrounds

There are many ways to detect FSK signals. However, both the direct-conversion and the frequency hopping features of our receiver architecture constrain the choice of the FSK detector. For a direct-conversion receiver, a quadrature baseband detector is required. Phase discontinuity which occurs when hopping excludes some types of FSK detectors. For a conventional superheterodyne receiver, IF FM detectors such as a limiter-discriminator [47] are typically used (Figure 3-29). However, this approach cannot be applied to our direct-conversion receiver. Simple flip-flop detectors or zero-crossing detectors [48] commonly used

![Figure 3-29 IF Limiter-Discriminator FSK Detector](image)

receiver. Simple flip-flop detectors or zero-crossing detectors [48] commonly used
in pagers with large modulation indices are not suitable for new digital wireless systems where bandwidth-efficient modulation implies only one signal cycle per baud.

Recently, new baseband detectors for binary FSK for the DECT and CT2 wireless standards have been proposed. In the approach followed in [49], the received I-Q signals are translated into corresponding magnitude and phase, and the difference between two consecutive phases is detected at the digital detector. Not only does this differential scheme require complex signal processing, but it is also limited to very low hop rate systems for the same reason as previously mentioned for DPSK (refer to Section 2.6.1). A balanced quotient detector is proposed in [50]; although it may be simple to implement, it is still analog in nature and has certain limitations. For example, clock recovery would be difficult, if not impossible, for a fast frequency-hopped receiver.

It is well-known that the optimum FSK detector is a correlation detector [15]. However, this detector is not often used in practice owing to the complexity of the required circuits. A simple multiplierless FSK correlation detector has been proposed for use in our frequency-hopped direct-conversion receiver.

**B. Multiplierless Correlation Detector**

In a sampled-data FSK correlation detector, the following correlation value \((CV)\) is evaluated for each tone:
where $\tilde{s}(nT_s)$ is the quadrature input signal, $f_t$ is the tone frequency to be detected, $T_s$ is the sampling clock period, and $N$ is the oversampling ratio ($T_{baud}/T_s$). This is in some sense equivalent to a Discrete Fourier Transform (DFT) technique, where a particular tone frequency is downconverted to DC, filtered by an integrate-and-dump (I&D) block, and its energy is detected. The magnitudes of the tone energies are compared, and the tone with the maximum correlation value is chosen as the transmitted tone.

A simple implementation for this algorithm has been sought. The quadrature input signals are first hard-limited using a limiting amplifier [51]. However, limiting introduces odd harmonics of the original tones. These harmonics are aliased after sampling, potentially corrupting the orthogonality of FSK tones applied to the digital correlation detector. However, it can be shown that the distortion due to harmonic aliasing is avoided if the oversampling ratio $N$ is chosen properly to guarantee that the generated harmonics are symmetric about half of the sampling frequency, retaining the Hermitian property of each I-Q signal. An integer multiple of eight (8i) for quaternary FSK and an integer multiple of four (4i) for binary FSK meet this requirement.

Figure 3-30 shows the correlation value plotted over different input frequencies for quaternary FSK: (a) for the ideal case and (b) for our detector. $N = 88$
was chosen, which implies roughly 7 MHz of the sampling clock (for $F_{sym} = 80$ kHz). Though it does not exactly mimic the ideal frequency discrimination plot, the curve for our detector still displays nulls at the desired tone frequencies. The detector must then only discriminate between signal energies at the tone frequencies of the set $\{ +2F_{tone}, +F_{tone}, -F_{tone}, -2F_{tone} \}$.

The input signal must be correlated with sine and cosine components for a quadrature correlator. Since the input signal is already hard-limited, the reference tone need not be a pure sinusoid. In our approach, square waves with the proper tone frequencies are used instead. Thus, an exclusive-NOR gate may be used as a one-bit multiplier for signal correlation. Harmonics resulting from the square waves can, after aliasing, downconvert undesired parts of the signal spectrum to baseband [52]. However, when the input signal is filtered and hard-limited, the
spectrum at the harmonics is due to the input signal itself. Thus, when the oversampling ratio constraint is met, there is no extra degradation.

The integrate-and-dump (I&D) block is implemented with a simple accumulator, and its clocks are generated by the clock recovery loop. As shown in (Eq. 3.14), the correlation detector also requires a magnitude calculation unit. In our architecture, an absolute-value addition block replaces a conventional squaring multiplier followed by a summing node. Thus, a truly multiplierless FSK detector is obtained with little performance degradation. The proposed quadrature correlator (Figure 3-31) is similar in topology to a butterfly unit of a DFT processor. It detects the correlation energy of the positive and negative tone pair ($\pm F_{\text{tone}}$).

![Diagram of Quadrature 1-bit Correlator]

Figure 3-31 Quadrature 1-bit Correlator

The architecture of the quaternary FSK demodulator (one branch only) is shown in Figure 3-32. It uses three such quadrature correlators: two for the two tone pairs ($\pm F_{\text{tone}}, \pm 2F_{\text{tone}}$) and a third for $\pm F_{\text{tone}}/2$, which is used as the frequency
error detector for the frequency tracking loop. The I-Q local tone generator is implemented with a one-bit output numerically-controlled oscillator (NCO), rather than a high-precision direct digital frequency synthesizer. The quadrature NCO generates I-Q $2F_{\text{tone}}$ square waves; the other local tones, $F_{\text{tone}}$ and $F_{\text{tone}}/2$, are produced by simple binary divisions of these. The reference tone frequency to be detected is fully programmable by controlling the input control word of the quadrature NCO.

![Multipllierless Quaternary FSK Detector](image)

**Figure 3-32 Multiplierless Quaternary FSK Detector**

### C. Implementation Loss

The implementation loss of our multiplierless FSK detector was studied via bit-level simulations. Simulation results showed about 1.2 dB of implementation loss for the quaternary FSK case in an additive white Gaussian noise (AWGN)
channel from the ideal full-precision correlation detector. In our detector, the Euclidean distance of the in-phase and quadrature components is approximated by summation of the two absolute values, thus eliminating squaring multipliers. Theoretically, this simplification results in a 3 dB magnitude degradation at the worst-case angle ($45^o$). A better approximation is suggested in [53]:

\[
\text{mag} = \begin{cases} 
  |i| + 0.5|q| & \text{if } |i| \geq |q| \\
  0.5|i| + |q| & \text{if } |i| < |q|
\end{cases} \quad (\text{Eq. 3.15})
\]

where $i$ and $q$ are the filtered quadrature components of the correlator. The maximum amplitude error is reduced to 0.97 dB at $26.6^o$. The degradation in our detector, though, is mainly due to the transient filter distortions aforementioned in

Figure 3-33  Implementation Loss of 1-Bit Correlation FSK Detector
Section 3.3.2.1. Given that the input signals are already hard-limited, the extra degradation due to one-bit signal correlation or absolute-value addition is minimal (about 0.1 dB), as shown in Figure 3-33. Therefore, the improved magnitude approximation scheme (Eq. 3.15) is not utilized. This keeps the baseband multiplierless FSK correlation detector simple, making it suitable for low-power direct-conversion applications employing FSK modulation.
Chapter 4

Baseband Processing Blocks

The remaining baseband processing blocks preceding the modulator or following the demodulator include a baseband controller which handles acquisition and frame synchronization in the receive mode, an interleaver/deinterleaver, a hop repeater/combiner, an optional channel coder/decoder, and an interface for voice and data. The baseband processing blocks developed for the proposed prototype handset are shown in Figure 4-1.

4.1 Sequential Hop Combiner

The proposed transceiver can handle various data rates between 2-160 kbps. When the (coded) data rate is lower than the modulation rate of 80 kbaud for quaternary FSK, the data may be repeated in symbol format. The repeat code is
ineffective in an AWGN channel [54]. It does, however, provide extra diversity over a Rayleigh fading channel when independent hops of the same information are combined after deinterleaving. For this sequential hop combining to work properly in a slow FH system, symbol interleaving is required rather than conventional bit interleaving. The repeater in the transmitter is realized by using an interleaver clocked at a rate \( R \) times faster than the symbol rate (\( R = 4 \) for our prototype). In the receiver, these \( R \) received symbol energies are combined using an I/D unit after deinterleaving.

Compared to antenna diversity, which can be thought of as a parallel diversity scheme, hop combining can be interpreted as a **sequential** diversity scheme.

![Baseband Processing Block Diagram](image-url)
(Figure 4-2). It should be noted that for a quaternary FSK system, symbol deinterleaving requires all four correlation values to be processed through both the
deinterleaver and the hop combiner before making decisions for the channel decoder input. This makes the baseband receiver slightly more complex; however, the hop combining gain obtained in this architecture is worth the penalty. For a fast FH system, the hop combining block precedes the deinterleaver, so simpler bit-level (de)interleaving can be used instead (Figure 4-3).
For sequential hop combining to be most effective, weighing each hop by relative Rayleigh magnitudes would be required. In a sense, this is equivalent to maximal-ratio diversity combining in a Rayleigh fading channel. Since accurate channel estimates are impossible in our frequency-hopped system, however, no attempt is made to estimate the channel parameters, providing only equal-gain combining gains.

In Rayleigh fading channels, the amount of diversity provided by a code is directly related to its minimum distance [15]. One way to increase the distance without increasing the constraint length of the code, which is exponentially proportional to the complexity of the decoder, is to repeat each output code $R$ times. The original minimum distance ($d_{\text{free}}$) is increased to $R * d_{\text{free}}$. This provides additional benefits even when repeat coding is combined with other efficient types of
convolution codes. However, the symbol interleaver/deinterleaver required for sequential hop combining in a slow FH transceiver results in a sub-optimal bit error rate performance, when combined with a typical binary code. This is due to the fact that symbol interleaving guarantees each hop to be independent only in a symbol fashion, not in a bit manner. In this scenario, nonbinary dual-k convolutional codes [15], which are designed especially for non-coherent M-ary modulations, can be used instead, thereby maintaining both optimal coding and hop combining gains.

4.2 Interleaver and Deinterleaver

An interleaving and deinterleaving technique often accompanies channel coding in order to randomize burst errors encountered in the channel [55]. The operation of block interleaving and deinterleaving is shown in Figure 4-4. At the

![Figure 4-4 Block Interleaving Operation](image-url)
transmitter, a sequence of data is written into the rows of the interleaver and read out in columns. At the receiver, the inverse process takes place: the data is written in columns and read out in rows. The size of the row should be big enough such that the corresponding time (in multiples of the symbol time) should be greater than the coherence time of the channel. The size of the column should also be greater than the decoding depth of the channel decoder. In a sense, this guarantees that the sequences of data are independent from one another over the decoding depth.

For a pedestrian communication link, the coherence time, which is inversely proportional to the Doppler frequency of the user in motion, is too long to be handled by this process. However, frequency hopping provides a unique scenario where fades in each hop become independent, provided that hop frequencies are separated by more than the coherence bandwidth of the channel and that the channel varies slowly with respect to the hop rate. Since our system is slow FH with 8 symbols per hop, a row size of 8 symbol periods satisfies this requirement. The column size has been chosen as 40 symbol periods for the proposed rate-1/2 Viterbi decoder [56].

There are two kinds of interleaving techniques: block interleaving and convolutional interleaving. A convolutional interleaver can be thought of as a block interleaver cut in half diagonally. The end-result of convolutional interleaving is the same as that of block interleaving, except its delay is half of the block inter-
leaver delay. The data stream is continuous, unlike block interleaving; therefore, no extra synchronization is required for convolutional interleaving. Since a hop frequency is applied diagonally (Figure 4-5), the hop phase jump is also randomized, unlike in block interleaving. Thus, the convolutional interleaving and deinter-

![Figure 4-5 Convolutional Interleaving Principle](image)

leaving technique is chosen over the block interleaving method for our architecture. An asymmetrical symbol interleaver/deinterleaver whose size is 8x40 can be built by using differently-sized delay elements (in multiples of 5) in each of 8 rows, as shown in Figure 4-6. The deinterleaver is more complex than the interleaver since total 12-bit information (3 bit times four tones) should be processed through, compared to only 2-bit information in the interleaver for 4-ary FSK. The overall delay of our interleaving and deinterleaving block is 280 baud symbols,
which corresponds to 3.5 ms for $T_{sym} = 12.5$ µs (80 kHz).

4.3 Baseband Controller

A baseband controller for the prototype handset which supports both data and voice services has been developed. Its first implementation in a field programmable gate array (FPGA) will handle only the simplex mode. It has four different modes of operation (Figure 4-7): initialization, self test, transmit, and receive. After power-up, the controller initializes the FSK modem settings and loads the coefficients for the synchronization loops. The self test mode is used only during testing. The receive states control the acquisition and reacquisition protocols, as well as the user interface in the receive direction. In the transmit mode, the con-
controller disables the demodulator and activates the frame counter. The interface between our transceiver and either the serial port (for data) or the FIFO (for the vocoder) is also controlled by this finite state machine.

4.4 Viterbi Decoder Interface

Since the data rate is relatively low, a node-serial architecture [57], in which a single add-compare-select (ACS) unit is time-shared between all states, is best suited for the proposed rate-1/2, constraint-length-6 Viterbi decoder. To maximize the coding gain, having soft-decision decoding capability is crucial. For binary FSK, the difference between the two correlation values ($CV$) can be used as soft decision metrics. The value of $\{CV(desired) - CV(undesired)\}$ for our 1-bit FSK detector is shown in Figure 4-8. Although it may not be exact, this value pro-
vides an indication of signal quality for different SNR scenarios to be used for branch metric calculations. For quaternary FSK, however, finding soft metrics becomes trickier. One efficient way is outlined in Figure 4-9, where $b_1$ and $b_0$ are the two inputs to the rate-1/2 Viterbi decoder. For the prototype FSK detector with an oversampling ratio of 88, the normalized maximum correlation value is only 0.688 (88/128). Therefore, the soft decision values should be renormalized to make the mean be 0.5 before actual quantization (to 3-4 bits precision).

4.5 User Interface

Both data and voice services are available for the FH/SS transceiver. A serial data port using a simplified RS-232 scheme provides an interface to a per-
sonal computer (PC) interface card. Both transmit and receive clocks are generated by the radio modem and enabled only during the appropriate frame slots. Various rates between 2-32 kbps are available for current wireless voice services [58], depending upon the type of vocoders being used. These include toll-quality adaptive delta pulse code modulator (ADPCM) for cordless systems and codebook exited linear predictive (CELP) techniques for low-rate digital cellular systems. Even the serial continuously-variable-slope-delta (CVSD) vocoder [59], whose operation is based upon an adaptive delta modulation technique, can be used to simplify the vocoder interface.

For our simplex prototype, a vocoder rate of 32 kbps was chosen. Since the

![4-FSK Metric Conversion](image)

\[
\bar{b}_1 = \max(Y_2, Y_3) - \max(Y_0, Y_1)
\]
\[
\bar{b}_0 = \max(Y_1, Y_3) - \max(Y_0, Y_2)
\]
data slots are only 80% of the frame, this implies that the minimum raw data rate be 40 kbps. This necessitates a buffer (FIFO) between the vocoder and the transceiver. The input/output timing and the size of the FIFO are dependent on the frame structure. In order to guarantee continuous transmission without emptying the buffer, the beginning of the transmit frame should be delayed accordingly, as shown in Figure 4-10. The size of FIFO should be at least the size of the data (C2)

![Block Diagram](image_url)

![FIFO vs. Frame Timing](image_url)

Figure 4-10 Transmit Vocoder FIFO Timing

slots as well. For the receiver, since the output rate (32 kHz) is slower than the received data rate (40 kHz) by the ratio of 4:5, proper operation is guaranteed as
long as the FIFO is clocked out after the first received data is written into the FIFO. The overall (one-directional) voice delay in our system, which is dominated by the delays in the transmitter buffer plus the interleaver/deinterleaver, is about 950 symbol cycles (< 12 ms for $F_{sym} = 80$ kHz). This delay is acceptable for voice services.
Chapter 5

Simulation

This section describes the simulation environment and methodology that are used for system performance and architecture trade-off studies. The overall system simulation block diagram is shown in Figure 5-1. An IF simulation model with dual receive branches which includes channel hopping effects has been developed. Two radio channel models are used. One is an additive white Gaussian noise (AWGN) channel for thermal noise, and the other is an independent flat Rayleigh fading channel. Given that the signal bandwidth is narrow and the hopping frequencies are separated more than the coherence bandwidth, this model represents a realistic situation that is frequently encountered in the radio microcellular environment. The AWGN channel in a sense represents the ideal channel where the radio has a direct line-of-sight (LOS) with negligible multipath; the Rayleigh model rep-
represents the worst-case channel where the frequency-hopped radio experiences frequency-selective flat fading. The actual channel scenario should be somewhere between these two extremes.

![Overall System Simulation Block Diagram](image)

Figure 5-1 Overall System Simulation Block Diagram

### 5.1 Simulation Environment

Simulations have been performed using both Signal Processing Worksystem (SPW) and Visual Analysis and Design Automation (VANDA) [60], an integrated CAD environment for communication signal processing systems being developed at UCLA. SPW is in general a time-driven simulator while VANDA is a data-flow simulator. Example schematics for both SPW and VANDA are shown in Figure 5-2 and Figure 5-3, respectively.
Figure 5-2  SPW Simulation Schematic (FSK Detector)

Figure 5-3  VANDA Simulation Schematic (Dual Diversity Receiver)
The data-flow simulator does not have any concept of time, and processes data whenever so-called tokens arrive at the input of the block. For the time-driven simulator, events in the simulation progress in every time step. The data-flow simulator is somewhat abstract since detailed clocking information is hidden. It is well-suited for multi-rate system simulations where perfect synchronization is assumed. For simulations in which clocking information such as sampling times are important or the clock rate is dynamically changing as in any tracking loop simulation, the time-driven simulator is effective. In general, the data-flow simulator is good for algorithm verification; the time-driven simulator works better for hardware architecture simulations. The scope of our simulations cover both system and hardware simulations. Though VANDA was used in some system simulations, most architecture simulations have been carried out using SPW. Matlab, a matrix processing software package from *The MathWorks*, was also used in some cases for simple algorithm verification and filter design. Simulation results are compared with analytical results whenever possible and presented in each section where appropriate.

### 5.2 SNR Estimator

The performance of a communications system is typically measured by the BER versus SNR. An SNR estimator is thus an important function. For an ideal FSK system, the SNR can be estimated by measuring two tone correlation values
(CV):

\[
SNR = \frac{CV(\text{desired tone}) - CV(\text{undesired tone})}{CV(\text{undesired tone})}
\]  
(Eq. 5.1)

The desired tone represents the signal power plus noise \((S + N)\), while the correlation value of the undesired tone indicates the noise level of the channel. The integrate-and-dump matched filter in the correlator determines the final noise bandwidth for an ideal FSK detector.

![Graph](image)

**Figure 5-4  SNR Estimation in Rayleigh Fading Channel**

For a high SNR case, the signal value itself is a good approximation to the actual SNR. The Received Signal Strength Indicator (RSSI) output with sufficient averaging (large time constant) can thus be used to estimate this value in an AWGN channel. In a fast-hopped system, though, this is not possible since the
channel is changing too fast. Although nonlinear hard-limiting makes accurate
SNR estimation difficult, the SNR calculated using the two tone values in our 1-bit
correlation FSK detector provides a rough approximation to the instantaneous
SNR (Figure 5-4).

5.3 Adjacent Channel Interference

The effects of multi-user interference were simulated using a simple model
in which other users occupy adjacent channel slots to the left and right of the
desired slot. Since neighboring channels are the dominant interferers, a scenario

![Multi-User Simulation](image)

Figure 5-5  Multi-User Simulation

with up to five users has been simulated. Because there is no explicit transmit
shaping filter employed in our FSK system, the spectrum leakage from the neigh-
boring channels degrades the performance. With four other adjacent users, the simulated SNR degradation, in a Rayleigh fading channel with $L = 2$, is about 1.7 dB from the single-user case at $10^{-4}$ BER. Up to a BER of $10^{-3}$, there is minimal degradation, probably due to orthogonality between the FSK tones (Figure 5-5).

5.4 Effect of Frequency Error

In our direct-conversion transceiver, the carrier frequency error could amount to ±100 kHz, assuming ±50 ppm crystal precision. The receiver therefore requires a means to compensate for this substantial frequency offset. In fact, the frequency offset problem is one of the serious challenges for implementing robust receivers for DECT or CT2. Since an analog FM detector is typically used to demodulate Gaussian FSK (GFSK) signals, the frequency error directly translates into a threshold voltage shift for the demodulated output for these receivers. Therefore, a complicated DC averaging scheme must be employed to handle this problem. Since DECT and CT2 utilize TDD as a duplexing scheme, the DC feedback loop becomes more complex in order to deal with the charge leakage occurring during the inactive time slots.

For our frequency-hopped FSK transceivers, however, frequency-offset compensation is done directly on the frequency-modulated signals using a very stable digital phased-locked loop. Figure 5-6 shows the behavior of the BER as a function of the SNR for different carrier frequency errors. The overall frequency
error should be less than 5 kHz to guarantee adequate performance.

Figure 5-6  Effect of Carrier Frequency Error
Chapter 6

Synchronization

Synchronization is important to establish a proper communication link between a transmitter and a receiver. The synchronization process can be divided into two general categories: acquisition and tracking. Acquisition refers to a process in which the receiver coarsely synchronizes the reference clock and carrier with the received clock and carrier frequency. Once acquisition has been achieved, the receiver needs to switch to a tracking process where it maintains its lock. Robust synchronization algorithms and architectures for master-slave configured frequency-hopped radios are described to acquire and track carrier frequency, time, and hopping codes.
6.1 Frame Structure

A simple frame structure with time-division duplexing (TDD) has been developed for transmitter and receiver synchronization, as shown in Figure 6-1.

![Figure 6-1 TDD Frame Structure](image)

The frame structure consists of a pilot tone (C0), a frame ID (C1), and actual data (C2). The C0 and C1 fields are for control slots and used in the acquisition process: C0 for energy detection and C1 for pattern matching (Word Sync). Their carrier frequency can be either fixed to a predefined acquisition frequency or hopped to a limited number of known frequencies. The acquisition time is shorter if the acquisition frequency is fixed since there is no need for sequential search. However, if the preassigned acquisition frequency receives interference or jamming for some unexpected reasons, a set of frequencies (even two) would be helpful to initiate a robust acquisition link. The carrier will of course be hopping during the C2 slots, where time and frequency are tracked.

Although the baseline modulation scheme is quaternary FSK, only binary
tones will be sent during the control slots (C0 and C1) to make acquisition easier. A dead zone (D) is inserted between the transmit and receive frames to account for the processing delay of the transceiver and the average propagation delay of the radio channel. The transceiver delay accounts for all of the filter and pipeline delays of the hardware. It is mainly dominated by the delay through the lowpass channel-select filter of the receiver, which is inversely related to the 3-dB corner frequency of the filter. For our system, this value corresponds to roughly 3 $\mu$s.

Given a maximum end-to-end distance of 500 meters in a peer-to-peer microcellular environment at 900 MHz, the propagation delay variation can amounts to 1.7 $\mu$s. This delay should be accounted for when switching between transmit and receive frames for a TDD system. Table 6-1 summarizes the data formats and operation of each field of the proposed frame.

<table>
<thead>
<tr>
<th>Field</th>
<th>Usage</th>
<th>Carrier Frequency</th>
<th>Data Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td>Frame (hop) synchronization, Coarse frequency acquisition</td>
<td>Fixed or Set of acquisition frequencies</td>
<td>2-FSK tones</td>
</tr>
<tr>
<td>C1</td>
<td>Receiver ID, Used for word sync (Barker code)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>Data slots, Time &amp; frequency tracked</td>
<td>Hopped</td>
<td>4-FSK tones</td>
</tr>
<tr>
<td>D</td>
<td>Dead zone to account for transceiver and link delays</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6-1 Frame Structure Summary

A typical frame length proposed for digital wireless systems ranges from 2
ms to 20 ms. The choice of the frame length trades off the overall link delay with the channel efficiency, which is defined as the ratio of control slots to the total number of frame slots. The shorter the frame, the shorter the link delay becomes. However, this implies a lower channel bandwidth efficiency since control signal overhead is required for acquisition and other functions. Since an overall transmission delay of 20-40 ms is acceptable for voice communication, a total frame length of 20 ms, 10 ms each for the transmit subframe and the receive subframe, is chosen. Thus, a 16-bit counter is sufficient for the frame counter for most scenarios with various data rates.

![Frame Structure Diagram](image)

**Figure 6-2** Detailed Frame Structure for Simplex Operation

The combination of C0, C1 and D slots compose 20% of the total frame slots. Thus, an 80% channel utilization can be achieved. For simplex operation of the prototype handset, the total of 20 ms is dedicated to either a transmit or a receive mode. This corresponds to a total of 1600 symbol slots for a symbol rate of
80 kHz for quaternary FSK, with 320 slots for control and 1280 slots for data. The
detailed frame structure for the simplex prototype handsets is shown in Figure 6-2.

6.2 Acquisition

Acquisition in time, frequency, and hopping code is accomplished by
means of frame synchronization. The control flow of this process is shown in Fig-
ure 6-3. It is achieved in two steps: coarse acquisition (energy detection) and fine
acquisition (pattern matching of the frame ID).

6.2.1 Coarse Acquisition

A purely digital Receiver Signal Strength Indicator (RSSI) detection
scheme using both energy detection and relative slope detection (Figure 6-4) cannot
be utilized since the hard-limiter eliminates absolute energy detection capabil-
ity in the digital domain. Moreover, the windowed, digital matched filter has a
sinc-shaped frequency spectrum associated with it. If the frequency offset pushes the tone frequency to the null locations, this scheme has no way of distinguishing the pilot tone. Therefore, the analog RSSI-aided energy detection scheme is used instead. In this scheme, the RSSI output, which is generated by a cascade of logarithmic amplifiers [51] after the channel-select filter, is used to coarsely indicate whether a C0 pilot tone is present or not. The slave handset first listens for the pilot

Figure 6-4  Digital Energy Detection Block Diagram
tone of the frame (C0) which is broadcast by the master on a pre-assigned acquisition carrier frequency.

The RSSI output is then compared to a programmable energy threshold value to produce either high or low output. This Signal Indicator Bit (SIB) indicates whether a signal is present at a particular acquisition frequency or not. The energy threshold voltage is generated by an 8-bit digitally controlled sigma-delta DAC, which is effectively an 8-bit accumulator followed by a pulse-width modulating lowpass filter (Figure 6-5). In theory, the threshold value can just be slightly above the noise level, since there is another level of security checked by the pattern matching logic. However, it should be set sufficiently high enough to optimize the total acquisition time by reducing the probability of false alarms.

Once the SIB goes high, frequency acquisition takes place by sweeping the frequency of the DDFS with a step size of $F_{\text{tone}}/4$ (20 kHz). The frequency sweep-
ing is required since the worst possible frequency error (±100 kHz) may be more than what the frequency tracking loop can handle. The 5-bit correlation value of a pre-determined tone (+F_{tone}) is evaluated to indicate a coarse frequency lock. Simulations have shown that a value of 17 out of the maximum possible 22 (for the case where the oversampling ratio N = 88) guarantees that the carrier frequency offset is within \( \pm F_{tone}/4 \) (20 kHz) from the desired (Table 6-2).

<table>
<thead>
<tr>
<th>( \Delta f )</th>
<th>-40 kHz</th>
<th>-20 kHz</th>
<th>0 Hz</th>
<th>+20 kHz</th>
<th>+40 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV (Max = 22)</td>
<td>12</td>
<td>20</td>
<td>21</td>
<td>18</td>
<td>14</td>
</tr>
</tbody>
</table>

Table 6-2 Correlation Value vs. Frequency Error

After coarse frequency acquisition, the rest of the C0 slots are used to detect a signal transition from +F_{tone} to -F_{tone}. The timing acquired during the C0 slots still has a \( \pm T_{baud} \) uncertainty associated with it since bit synchronization has not been yet achieved. Therefore, the received data needs to be matched with the unique ID pattern before frame synchronization is declared. Once frame sync is declared, the receiver starts demodulating data. The hopping code synchronization relies on the fact that once the frame is synchronized, a pre-defined frequency hopping pattern is repeated every frame. Thus, no extra pseudo-noise (PN) code acquisition is required as in a DS system.

The acquisition time for an serial search method for a DS system with a \( T_c/2 \) sliding correlator can be shown to be [15]
\[ T_{acq} = \frac{T_u}{T_c} \cdot NT_c = 2NT_u \text{ (sec) } \]  

(Eq. 6.1)

where \( T_u \) is the initial timing uncertainty, \( T_c \) is the PN chip duration, and \( NT_c \) is the examination time, which should be ideally an integral multiple of PN code words to take full advantage of the autocorrelation properties of the PN sequence. This implies that the C0 field must be at least \( 2NT_c \) seconds long for the receiver to have sufficient time to search in a serial fashion. Since a long PN code sequence is typically employed in a DS transceiver, this can be a bottleneck [61]. Alternatively, a parallel search method can be used in order to reduce the acquisition time. However, this requires a more complex and costly implementation utilizing parallel matched filters. Compared to a DS system, the proposed wake-up tone scheme for synchronous-access frequency-hopped transceivers is much simpler and relatively faster.

The hop time synchronization is performed in an open-loop fashion as explained in Section 3.3.2. The time constant (\( \tau \)) of the RSSI and the lock time of the baud and frequency tracking loops affect the length of each field in the frame. For instance, the time constant should be large enough such that the RSSI value can average the instantaneous signal variations. With an increasing value of \( \tau \), however, the length of the control field (C0) is also increased, since it should be at least a few times larger than the value of \( \tau \) in order to provide sufficient detection time. The RSSI time constant must be limited to a value of less than 500 \( \mu \text{s} \) for this
6.2.2 C1 Pattern Recognizer

Pattern matching of the C1 code is required for group synchronization (or frame synchronization). A 21-digit binary Barker code [62] is used for this purpose. It has the autocorrelation characteristic shown in Figure 6-6. The Barker code is somewhat similar to the M-sequence code, often used as a spreading code in DS systems. The number of positive one’s and negative one’s only differs by one. The autocorrelation value peaks when the reference and received codes align; otherwise, its value is quite small. Rather than having 21 independent digits, the pattern consists of three subsets of a seven-digit code \{1 1 1 -1 -1 1 -1\}: the first two sets have a positive polarity and the third one has a negative polarity. This way, the number of fan-ins to the summing adder can be substantially reduced. The maximum correlation value is +21; therefore, a 5-bit programmable threshold value

![Figure 6-6  Autocorrelation of 21-Digit Barker Code](image)
is sufficient. The block diagram of the C1 pattern recognizer is shown in Figure 6-7.

Simulation results have shown that a threshold of 16, which allows two random errors in the pattern, is a reasonable choice to declare a pattern match (Figure 6-8). Even with 15 dB of SNR, this threshold was able to discriminate the pattern from noise. The peak value was 17 while the next highest value near the symbol digit (within ±4 symbol durations) was only 3 with the following conditions: timing phase error \( T_{err} = T_{baud}/4 \) and frequency error \( F_{err} = F_{baud}/8 \) (10 kHz). Alternatively, a threshold of 18 can be used if a tighter acquisition condition (for example, \( T_{err} = T_{baud}/8 \) and \( F_{err} = F_{tone}/16 \)) is required. Since a coarse acquisition is achieved by detecting the signal transition at a pre-defined location in the C0 field, the pattern matching process can be enabled only over a certain window.
period, for example plus or minus four baud cycles around the expected time instant. This makes the fine acquisition process more robust and a 21-digit pattern sufficient for our purpose.

![Pattern Matching Simulation](image)

6.2.3 Reacquisition

A reacquisition process is required when the receiver loses its lock temporarily due to long time-selective fading such as ducting or tunneling. Figure 6-9 shows a timing diagram which explains the acquisition and reacquisition process with the frame time line. Only receive frames are shown for simplicity and the fields are not drawn to scale. The down-arrow inside the frame represents a signal
transition from $+F_{\text{tone}}$ to $-F_{\text{tone}}$ during the C0 slots, while the up-arrow symbolically indicates the end of the C1 ID pattern. After the SIB goes high for a while, a signal transition is detected, indicating a coarse acquisition. This enables the receive frame counter, which in turn generates a pattern-match window at the proper time. The frame resets itself and generates a pulse where it thinks the pattern match should occur. The pattern match signal detected by the C1 recognizer, though, overrides the one generated by the frame counter, resetting the frame counter. If no match is detected over the windowed period by the pattern recognizer, the synchronization circuit generates a miss. If more than five consecutive misses are reported, the receiver goes through a reacquisition process and the entire synchronization process starts over. A more detailed control flow diagram
for the synchronization process is shown in Figure 6-10.

6.3 Tracking

The acquisition process only guarantees the accuracy of the baud clock and the carrier frequency to within a reasonable range of error. It is thus up to the time and frequency tracking loops to pull in the remaining errors and maintain lock. A tracking loop requires phase-locked loop (PLL) techniques whose implementation
can be completely analog, digital, or a combination of both. Before actually describing our time and frequency tracking loops, various loop architectures are first discussed and compared.

### 6.3.1 Loop Architectures

Generally speaking, a PLL consists of three major components: a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO). The PD is a key component in the PLL and its implementation varies depending on the application. A systematic categorization of various PDs is undertaken in [63]. Four distinct classes of PDs are as follows: flip-flop PD, Nyquist-rate sampling PD, zero crossing PD, and lead-lag (or early-late) PD. The loop filter works as a lowpass filter, averaging out instantaneous phase errors in the loop. An active analog implementation of the first-order loop filter is shown in Figure 6-11(a), while its digital implementation is shown in Figure 6-11(b).

![Figure 6-11 First-Order Loop Filters](image)

**Figure 6-11 First-Order Loop Filters**
counterpart is shown in Figure 6-11(b). For an analog filter, the values of resistors and capacitors determine two time constants ($\tau_1$, $\tau_2$), which in turn affect the natural frequency ($\omega_n$) and the damping factor ($\zeta$) of the loop [64]. For a digital filter, the values of the linear coefficient (K0) and the integrator coefficient (K1) determine both the loop gain and the loop bandwidth (Figure 6-12). Two other types of the digital loop filter are also available (Figure 6-13).

A VCO can be modeled as an integrator. For a digital PLL, a DDFS replaces the VCO in the carrier recovery loop and an NCO substitutes for the voltage-controlled crystal oscillator (VCXO) for a clock recovery loop. The speed of the clock is one of the factors that impact the trade-off between digital and analog implementations of the VC(X)O. For example, if the required output clock rate is
too high (> 10 MHz), the time recovery loop is typically implemented using an analog VCXO rather than an NCO. The (maximum) phase jitter of the NCO is directly related to the sampling clock rate ($F_{clk}$). $F_{clk}$ should be at least 20-30 times higher than the nominal output frequency in order for the loop not to be limited by the clock phase jitter. This makes an NCO implementation impractical. Therefore, for a high clock rate (or a high-frequency DDFS), a mixed PLL design is required, necessitating a high-resolution DAC.

A one-bit sigma-delta DAC implementation can simplify this interface (Figure 6-14). The carry-out bit of an N-bit accumulator is fed into the pulse-width modulating lowpass filter. The rate of overflow determines the output voltage level variation from the nominal value ($V_{nom}$). Note that the loop filter is clocked with period $T_{sym}$ and its signal values are represented in two’s-complement numbers,
while the “unsigned” accumulator is sampled with $T_{clk}$. A “0” output of the loop filter (in two’s complement notation) corresponds to $V_{nom}$ at the output of the LPF. A plus or minus value of the LF output is thus translated into $\{V_{nom} \pm dV\}$. The corner frequency of the LPF should be set to encompass the bandwidth of the sigma-delta input (jitter) rate. The oversampling ratio ($OR$) between $F_{clk}$ and $F_{sym}$ improves the noise performance of this first-order sigma-delta DAC, effectively making it $\log_2(OR)$ bits wide.

If a DDFS technique is used for carrier generation, as in digital IF receivers, a fully digital loop architecture is appropriate. Since the DDFS is used for hopping carrier generation and the baud clock frequency is relatively low (80 kHz) in our system, both the time tracking and the frequency tracking loops have adopted a fully digital-PLL architecture. Figure 6-15(a) shows a block diagram of the typical second-order digital PLL architecture. A version using a prescaler is shown in Fig-

Figure 6-14  Mixed-Signal Domain PLL with Sigma-Delta DAC
ure 6-15(b). Both loop architectures are functionally identical, except that the latter allows a reduced internal wordlength and thus a smaller size adder in the loop filter. The prescaler value $2^K$ limits the maximum range of the instantaneous frequency deviation from the nominal value stored in the offset register. This prescaler architecture might be useful in some applications, such as in the PN tracking loop of a direct-sequence receiver, where the loop clock rate is relatively high. Since the loop typically operates at the symbol rate, speed is not a bottleneck; therefore, a normal loop architecture without the prescaler is suitable in general.
Moreover, with this architecture the nominal output frequency control word can be directly loaded to the integrator register in the loop filter since the full wordlength is used. This simplifies the I/O requirements.

Another type of loop that is frequently used in clock recovery for high-speed data transmission systems is a delay-locked loop (DLL). Rather than changing the frequency of the VCO (or VCXO), the DLL only allows phase changes of a poly-phase ring oscillator to lock on to the correct phase of the received clock (Figure 6-16). The loop filter (integrator part only) is often replaced by an up/down counter for simplicity. Only small frequency errors can be recovered here. This loop architecture is not considered in our time tracking loop design since an analog ring oscillator is required. It is mostly suitable for high-speed data communications systems with up to 100 MHz output clock rates where the frequency offset between the transmitter and the receiver is negligible.

Figure 6-16  Delay-Locked Loop Architecture
6.3.2 Time Tracking Loop

The time tracking loop (TTL) consists of a PD, a loop filter, and an NCO (Figure 3-24 in Section 3.3.2). An early-late phase detection scheme is used to generate a phase discriminant. The correlation energy of the first-half symbol minus that of the second-half symbol is detected for each tone and the output from one of the four tones, chosen by the hard decision bits, is fed into the loop filter. For the PD output, four-bit quantization with the rounding scheme is chosen over one-bit hard decisions since soft decisions reduce the phase jitter for the same set of coefficients when a stable condition is reached. Both filter coefficients K0 and K1 have programmable powers-of-two coefficients so that the loop can handle various tracking ranges depending on the required clock jitter of the overall system. The loop architecture is simplified by replacing an expensive digital multiplier with an add-and-shift operator and limiting the number of coefficient choices to only eight. The set of coefficients was carefully chosen by simulation. Table 6-3 shows the set of chosen coefficients for both K0 and K1.

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>K0</td>
<td>$2^{-7}$, $2^{-8}$, $2^{-9}$, $2^{-10}$, $2^{-11}$, $2^{-12}$, $2^{-13}$, $2^{-14}$</td>
</tr>
<tr>
<td>K1</td>
<td>$2^{-15}$, $2^{-16}$, $2^{-17}$, $2^{-18}$, $2^{-19}$, $2^{-20}$, $2^{-21}$, $2^{-22}$</td>
</tr>
</tbody>
</table>

Table 6-3 TTL Loop Filter Coefficients

When the data is not changing, the output of the PD should be theoretically
zero. The loop is thus enabled only when symbol transitions occur during the C2 slots of the receive frame. For the case where only one antenna branch is active, an autoscaler for the PD is used to guarantee the same loop gain as in the dual antenna case. A 24-bit internal wordlength is chosen for the loop filter. The NCO logic thus uses a 24-bit accumulator, which results in a 0.5 Hz tuning resolution at a 7.15 MHz demodulator clock rate.

An “S-curve” is used to measure the quality of the PD algorithm. Our FSK demodulator uses only one-bit signal correlation, and the magnitude calculation is performed by summation of two absolute values. Due to these simplifications, the PD S-curve deviates from the ideal case. Unlike its ideal counterpart, the shape of the S-curve varies depending on the carrier phase offset. One-bit approximation

![Figure 6-17 TTL S-Curve for Carrier Phase Offset = π/4](image)

Figure 6-17  TTL S-Curve for Carrier Phase Offset = π/4
results in a flat region in the middle of the S-curve (Figure 6-17). Intuitively, this phenomenon can be explained by taking the early-late PD output of the two coherent, real square waves. Until there is a sufficient timing offset, there is no way to differentiate phase variations. The absolute-value magnitude calculation also results in a dead zone at the edges of the curve. However, when the PD output is averaged over different carrier phases, simulation results have shown that the shape of our S-curve closely resembles that of the ideal one (Figure 6-18). Due to an inherent frequency offset between the transmit and receive carriers, the loop tends to rotate around all carrier phases until it locks. Furthermore, the channel-select lowpass filter averages out different phases. Therefore, this carrier phase-averaged scheme is acceptable for our receiver.

![Figure 6-18 Phase Error Detection of TTL](image)

(a) Detection Algorithm
(b) S-curve
Figure 6-19 shows an example of the TTL simulations. The loop filter output trajectory is shown as the number of baud intervals increases for a worst case condition with a phase error of 180 degrees and a clock frequency error of 250 Hz (~3000 ppm with respect to $F_{sym} = 80$ kHz). Two different sets of coefficients are used for acquisition: an initial wide loop bandwidth and a narrow loop bandwidth for final tracking. A steady-state condition (or lock) is accomplished in about 500 baud cycles and the loop is switched to a tracking mode at about the 1600th baud cycle.

![Figure 6-19   TTL Loop Filter Output Trajectory](image)

| WB | K0 = $2^{-10}$  
|    | K1 = $2^{-18}$  
|    | (Acquisition)  
| NB | K0 = $2^{-12}$  
|    | K1 = $2^{-21}$  
|    | (Track)        

6.3.3 Frequency Tracking Loop

For the frequency tracking loop (FTL), a frequency detector (FD) replaces the phase detector and a high-precision DDFS is used instead of a one-bit NCO
(Figure 3-24 in Section 3.3.2). The difference between the two correlation energies at frequency nulls of the $+F_{\text{tone}}$ and $-F_{\text{tone}}$ data can be used as the FD output; however, this provides a lower overall loop gain (Figure 6-20). Thus, it is not selected.

Instead, the difference between the two correlation energies at $+F_{\text{tone}}/2$ and $-F_{\text{tone}}/2$ is used as the baseline frequency discriminator. When a signal with either $+F_{\text{tone}}$ or $-F_{\text{tone}}$ is received, its correlation value is stored and compared with the other correlation value. The 4-bit FD output is then fed into the loop filter only when a transition from $+F_{\text{tone}}$ to $-F_{\text{tone}}$ or vice versa occurs. This scheme simplifies the frequency error detection block significantly and thus justifies its usage in our FTL.
Since the FTL only requires a first-order loop, the linear path is not necessary. The eight chosen loop coefficients are listed in Table 6-4. The loop filter has a 24-bit internal wordlength. The input frequency control word of the DDFS has been chosen to be 24 bits wide as well. Although the simulation shows a 20-bit implementation would have been sufficient, this choice fully utilizes the precision of the loop filter output and guarantees a 5 Hz frequency tuning capability at a DDFS clock rate of 76 MHz.

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>K1</td>
<td>$2^{-14}, 2^{-15}, 2^{-16}, 2^{-17}, 2^{-18}, 2^{-19}, 2^{-20}, 2^{-21}$</td>
</tr>
</tbody>
</table>

Table 6-4  FTL Loop Filter Coefficients

Due to hardware simplifications for the FSK detector, the FD S-curve

Figure 6-21  Frequency Error Detection of FTL

Due to hardware simplifications for the FSK detector, the FD S-curve
results also depend on the carrier phase offset. Again, the phase-averaged scheme shows acceptable characteristics (Figure 6-21). Statistically speaking, the loop is activated only in one out of eight clocks due to the data transition restriction in our FD scheme, thus slowing down the frequency tracking process. Figure 6-22 shows a simulation example with a frequency error of 20 kHz ($F_{\text{tone}}/4$). Acquisition is achieved in about 1000 baud cycles. To speed up the tracking process, the difference between two correlation values at $+3F_{\text{tone}}/2$ and $-3F_{\text{tone}}/2$ can also be used; however, this scheme requires more complex circuits, especially since the $3F_{\text{tone}}/2$ tone cannot be generated by simple binary division from the $2F_{\text{tone}}$ reference tone. Thus, it is not utilized.

![Figure 6-22  FTL Loop Filter Output Trajectory](image)

\[ WB = K_1 = 2^{-15} \quad (\text{Acquisition}) \]

\[ NB = K_1 = 2^{21} \quad (\text{Track}) \]
6.4 Digital PLL Analysis

In this section, a digital PLL is analyzed in detail. Analog PLLs have been studied in detail [64], [65], [66]. Some results drawn from the known analog PLL analysis are applied to the digital PLL case. A typical continuous-time PLL block and its linearized model are shown in Figure 6-23, while its discrete-time counterpart is shown in Figure 6-24. (Eq. 6.2) and (Eq. 6.3) represent the closed-loop transfer function for continuous-time and discrete-time linearized PLLs, while (Eq. 6.4) and (Eq. 6.5) show the transfer function of the error output to the input phase error for the same loops.

\[ H(s) = \frac{\Theta_a(s)}{\Theta_i(s)} = \frac{K_d F(s) N(s)}{1 + K_d F(s) N(s)} \]  
\[ (Eq. 6.2) \]

\[ H(z) = \frac{\Theta_a(z)}{\Theta_i(z)} = \frac{K_d F(z) N(z)}{1 + K_d F(z) N(z)} \]  
\[ (Eq. 6.3) \]
$K_d$ represents the PD gain, whose units are in volts/radian for the analog PLL. For the direct digital analysis, it can be represented as an actual value in $[-1, 1)$. The VCO can be modeled as an ideal integrator with the gain constant $K_o$. For example, the output frequency ($f_o$) of the VCO can be represented as

$$f_o = K_o \cdot v + c$$  \hspace{1cm} \text{(Eq. 6.6)}$$

where $K_o$ is in units of Hz/volt. For the digitally-controlled oscillator (DCO), $K_o$ is often represented as Hz/LSB.

The steady-state error performance can be analyzed using the error transfer function. The steady-state error of the loop as time approaches to the infinity can be calculated using the error transfer function $H_e(s)$:

$$H_e(s) = \frac{\Theta_e(s)}{\Theta_i(s)} = \frac{1}{1 + K_d F(s) N(s)}$$  \hspace{1cm} \text{(Eq. 6.4)}$$

and

$$H_e(z) = \frac{\Theta_e(z)}{\Theta_i(z)} = \frac{1}{1 + K_d F(z) N(z)}$$  \hspace{1cm} \text{(Eq. 6.5)}$$
be found by evaluating $H(s)$ as $s \to 0$ or $H(z)$ as $z \to 1$, according to the final value theorem. A pole at DC can be shown to be required to null out the error. The order of the denominator of the closed-loop transfer function determines the order of the PLL. When an $m^{th}$-order loop filter is used within the loop, the overall phase-locked loop is $(m+1)^{th}$-order. For example, the most popular second-order loop can completely correct for both phase errors and small frequency offsets, while the first-order loop can only handle for phase errors.

The closed-loop response can be used to find the loop bandwidth. From (Eq. 6.2) and (Eq. 6.3), it can be deduced that the loop bandwidth of the first-order system depends only on the DC loop gain ($K_v = K_d \cdot K_o \cdot K0$). For the second-order system, however, it is more complicated since the loop bandwidth is a function of both the natural frequency ($\omega_n$) and the damping factor ($\zeta$). The relationship between the analog and digital PLLs has been derived for an ideally linearized second-order PLL model [67]:

$$\frac{K0}{K1} = \frac{2\zeta}{T\omega_n} \quad (Eq. 6.7)$$

where $T$ is the sampling clock. This mapping was achieved using the bilinear transform technique in the frequency domain. This equation gives a relation between the ratio of $K0/K1$ and the loop bandwidth; however, it does not provide much insight on choosing the actual values of $K0$ and $K1$ with respect to the loop
bandwidth. Actual coefficient values thus need to be determined by means of simulation.

Another method based on the direct time-domain analysis is derived to determine the values of the loop filter coefficients with respect to the loop bandwidth. The system rise time (10% to 90%) of the loop corresponding to the step response is evaluated in terms of the symbol time. The following relationship [68] is then used to determine the loop bandwidth of the digital loop:

\[ T_r = \frac{2.2}{2\pi f_L} = \frac{1}{\pi f_L} \]  \hspace{1cm} (Eq. 6.8)

where \( T_r \) is the rise time and \( f_L \) is the 3-dB closed-loop bandwidth. A shorter rise time is desired for the faster dynamics of the loop; however, a smaller \( f_L \) is required to reduce the effective noise bandwidth, which is roughly the same as the loop bandwidth. This implies that both conditions cannot be satisfied at the same time; rather, a trade-off should be sought out to find the optimum operating point.

### 6.4.1 First-Order Digital Loop Analysis

For the first-order loop, the loop filter \( F(z) \) has only a constant term \( K_0 \). Since the typical loop is updated in every symbol time, the system rise time in the linearized PLL model can be represented as

\[ T_r = \frac{\phi(err)}{\phi(T_s)} \cdot \frac{T_s}{K_d} \]  \hspace{1cm} (Eq. 6.9)

where \( \phi(err) \) refers to the step phase error, \( \phi(T_s) \) corresponds to the phase error that
can be corrected in each symbol duration, and $K_d$ is the normalized PD output whose average value is 1/2. An assumption made here is that the system is ideal and noiseless. The delays in the loop do not affect the system rise time, although they may affect the overall acquisition time and stability. When the loop is enabled during data transitions, for example, the total acquisition time is at least

$$T_{acq} = T_{dly} + p \cdot T_r$$

(Eq. 6.10)

where $p$ is the probability of transition between (0, 1].

![Figure 6-25 NCO Operation](image)

For the first-order time tracking loop (TTL), the maximum phase error is $\pi$, which corresponds to a phase offset of $T_s/2$. Since the input of the NCO is the input frequency control word, it is easier to calculate $T_r$ in terms of frequency
rather than phase. Assuming the operation of the NCO shown in Figure 6-25, phase can be mapped linearly into frequency:

\[ \phi = \int K_0 df = K_0 \cdot f \]  

(Eq. 6.11)

Therefore, the phase advance per symbol can be represented as

\[ \phi (T_s) = K_0 \cdot F(K0) \cdot N \]  

(Eq. 6.12)

where \( F(K0) \) is the instantaneous frequency corresponding to the value of K0 in the loop and \( N = F_{clk}/F_{sym} \). This represents an incremental movement per baud \((\Delta T)\) in the time line. Since

\[ \pi = K_0 \cdot F_{sym} \cdot \frac{N}{2}, \]  

(Eq. 6.13)

the system rise time is given as

\[ T_r = \frac{F_{sym} \cdot T_s}{F(K0) \cdot 2K_d} = \frac{1}{2K_d \cdot F(K0)}. \]  

(Eq. 6.14)

From (Eq. 6.8), the loop bandwidth of the first-order TTL is

\[ f_L = \frac{F(K0)}{\pi}. \]  

(Eq. 6.15)

The average value of \( K_d \) is assumed to be 1/2 for the ideal case. Figure 6-26 shows the closed-loop transfer function \( H(z) \) for different values of K0. As expected, the 3-dB loop bandwidth is reduced as the value of K0 decreases.

The delays in the loop affect the stability of the loop. Figure 6-27 shows the closed-loop response for the first-order loop with different delays. The loop band-
width of the simulated case is about $F_{\text{baud}}/20$. With an increasing number of delays, peaking occurs around the corner frequency, worsening the phase response. Finally, when the number of delays is more than 5, the loop becomes unstable.

### 6.4.2 Second-Order Digital Loop Analysis

For the second-order digital PLL, the loop filter block (Figure 6-11(b)) has two programmable coefficients: the linear term ($K_0$) and the integrator term ($K_1$). The linear term provides instantaneous frequency offsets to the DCO, thus correcting the phase offset between the transmitter and receiver, while the integrator path can actually provide a frequency offset in the integrator to compensate for the frequency errors in the system. Although it might not be rigorous, the direct time-
domain analysis technique using the system rise time argument can also be applied to gain some insights into the values of K0 and K1 relative to the loop bandwidth.

Figure 6-27  Closed-Loop Response with Delays
The rise time for the ideal case for a given frequency error $F(\text{err})$ is

$$T_r = \frac{F(\text{err})}{F(K_0)} \cdot \frac{K_0}{K_1} \cdot \frac{T_s}{K_d} \quad \text{(Eq. 6.16)}$$

where $\frac{K_0}{K_1} \cdot T_s$ represents the time it takes for the integrator to accumulate the frequency offset corresponding to $F(K_0)$.

Ideally, the linear term should not affect this integration process since it only handles the phase offset. To correct the total frequency error, this time should be multiplied by $F(\text{err})/F(K_0)$. Relating to (Eq. 6.8), the loop bandwidth is then

$$\hat{f}_L = \frac{F_{\text{sym}}}{(K_0/K_1)} \cdot \frac{K_d F(K_0)}{F(\text{err})} \quad \text{(Eq. 6.17)}$$

The maximum frequency error that the loop can correct is defined as the “pull-in range” or the “acquisition frequency” of the loop $F(\text{acq})$ [64]. When $F(\text{err}) = F(\text{acq})$, (Eq. 6.17) can provide a heuristic to find the appropriate values of K0 and K1. The value of K0 should be chosen such that $F(K_0)$ is equal or slightly higher than $F(\text{acq})$. This choice is based on the fact that $F(K_0)$, which represents the instantaneous tracking frequency range, should be comparable to the value of the frequency error in order for the loop to have an adequate gain. The ratio $K_0/K_1$ should also be chosen so that the final value of the frequency jitter, which is controlled by the value of K1 after acquisition, is small compared to $F(\text{err})$ or $F(K_0)$. If the value of $F(K_0)$ is chosen relatively high compared to $F(\text{err})$, the value of the ratio should be made larger in order to provide the same rise time and thus the
same loop bandwidth.

The damping factor of the loop is ignored in this analysis; however, it is embedded in the process of choosing the appropriate values of K0 and K0/K1. For instance, when $F(err) = F(acq)$, a small value of K0/K1 ($< 10$) is equivalent to having a underdamped condition with a fast acquisition but with a greater error. When the value of the ratio is higher ($> 1000$), this corresponds to an overdamped situation with a very small steady-state error but with a longer acquisition time.

For a typical case where $F(K0) = 2^*F(err)$ and $K_d = 1/2$, (Eq. 6.17) simplifies to

$$f_L = \frac{F_{sym}}{(K0/K1) \cdot \pi}$$

(Eq. 6.18)

which is equivalent to (Eq. 6.7), assuming $f_L = \omega_n / 2\pi$ and $\zeta = 1$. Two important conclusions drawn from this analysis are as follows:

- K0 affects the loop gain of the digital PLL; and
- the ratio K0/K1 mostly determines the loop bandwidth and the damping factor.

### 6.4.3 Frequency-Locked Loop

A second-order PLL is typically employed in a receiver where both phase and small frequency offset errors need to be corrected. The Costas loops used in phase- or amplitude-modulation receivers are one such example. However, the total frequency offset that can be corrected is limited by the delays in the loop.
When the frequency offset is relatively large, as in this FH system, a frequency-locked loop (FLL) is required rather than a PLL. The digital FLL consists of a frequency detector (FD), a loop filter, and a DDFS (Figure 6-28). The maximum frequency error it can correct is now limited by the S-curve characteristics of the frequency detector, typically up to half of the symbol rate. The DDFS in this case just maps the input frequency to the output frequency with a linear gain $K_o$. Since the VCO is no longer an integrator, a loop filter with only the integrator term is required to average out the instantaneous frequency errors. The overall loop is thus first-order. The system rise time in the linearized model is expressed as

$$T_r = \frac{F(\text{err})}{F(K1)} \cdot \frac{T_s}{K_d}$$  \hspace{1cm} (Eq. 6.19)

where $F(\text{err})$ is the maximum error of the loop and $F(K1)$ is the amount of frequency offset that the loop can correct per symbol duration. Thus, the
corresponding loop bandwidth is

\[ f_L = \frac{F_{\text{sym}}}{F(\text{err})/F(K1)} \times \frac{K_d}{\pi} \]  

(Eq. 6.20)

### 6.4.4 Effect of Oversampling Ratio

The DCO (either DDFS or NCO) gain \( K_o \) can be represented in units of Hz/LSB. For the fixed loop wordlength, this implies that \( K_o \) becomes bigger as the DCO clock rate gets higher with respect to the symbol rate. This increases the overall loop gain. In order to maintain the same gain, this forces the values of the loop filter coefficients (\( K0 \) and \( K1 \)) to scale down with an increasing DCO clock rate. Otherwise, the loop wordlength should be increased accordingly to maintain the same NCO gain in Hz/LSB. Table 6-5 shows the time and frequency tracking loop coefficients for our FH/SS transceiver for different clock rates. The results confirm our assumption.

<table>
<thead>
<tr>
<th></th>
<th>TTL</th>
<th>FTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>F(err)</td>
<td>( F_{\text{NCO}} = 5 ) MHz</td>
<td>( F_{\text{err}} )</td>
</tr>
<tr>
<td></td>
<td>( F_{\text{NCO}} = 10 ) MHz</td>
<td>( F_{\text{DDFS}} = 40 ) MHz</td>
</tr>
<tr>
<td>250 Hz</td>
<td>( K0 = 2^{-9} )</td>
<td>( K0 = 2^{-10} )</td>
</tr>
<tr>
<td></td>
<td>( K1 = 2^{-17} )</td>
<td>( K1 = 2^{-18} )</td>
</tr>
<tr>
<td></td>
<td>( K1 = 2^{-15} )</td>
<td>( K1 = 2^{-16} )</td>
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<td>1 kHz</td>
<td>( K0 = 2^{-8} )</td>
<td>( K0 = 2^{-9} )</td>
</tr>
<tr>
<td></td>
<td>( K1 = 2^{-15} )</td>
<td>( K1 = 2^{-16} )</td>
</tr>
<tr>
<td></td>
<td>( K1 = 2^{-14} )</td>
<td>( K1 = 2^{-15} )</td>
</tr>
</tbody>
</table>

Table 6-5 Loop Coefficients vs. Clock Rates
6.4.5 Quantization Effect of Phase Detector

The PD output in reality is quantized as either one-bit hard decisions or three- to four-bit soft decisions. For the hard-decision (HD) case, the shape of the ideal S-curve will be abrupt around the zero phase reference. Taking noise into account, however, the averaged S-curve shape shows a similar characteristic to that in the soft-decision (SD) case. For a given set of loop filter coefficients (K0, K1), the loop with hard decisions locks to a stable condition much faster since it has an effectively higher PD gain ($K_d$). In the steady state, however, it generates much more jitter than the SD case because the instant PD error is higher.

In order to reduce the phase jitter, the values of the filter coefficients should be made smaller, which implies a longer acquisition time. The total loop word-length is effectively the same as in the SD case, since smaller coefficients require longer wordlengths. The best compromise would be to a soft-decision PD output and control the speed of acquisition by changing the loop filter coefficients. This way, one can achieve acquisition relatively fast with a set of large initial coeffi-

![Phase Detector Rounding Scheme](image)

Figure 6-29  Phase Detector Rounding Scheme
cients and also have a relatively small steady-state jitter once locked.

For PD quantization, either rounding or truncation schemes can be applied. The rounding scheme requires a half-least significant bit (LSB) to be added before actual quantization (Figure 6-29). The truncation scheme simplifies the PD generation block since no extra adder is required. However, a half-LSB bias inherent in the truncation scheme could introduce a significant error (Figure 6-30), especially during the initial acquisition process where the loop coefficients are relatively large. For the first-order TTL, this implies the following phase bias:

\[
\frac{2\pi \cdot F(0.5 \cdot 2^{-L} \cdot K0)}{F_{sym}}
\]

(Eq. 6.21)

where \( L \) is the number of PD quantization bits and \( F(*) \) implies the instantaneous frequency of the DCO corresponding to the input value. This phase error may or

Figure 6-30  PD Quantization Bias
may not be acceptable, depending on the value of K0. The rounding scheme has a zero bias; thus, this problem is eliminated by using rounding.

6.5 Multi-User Synchronization

So far, synchronization studies have been limited to a peer-to-peer communication link. For multi-user scenarios, a (micro)cellular structure where all users communicate through a base station would be possible (Figure 6-31(a)). Of course, network synchronization between the users in the cell (as well as neighboring base stations) must be coordinated carefully so that the synchronous FH-CDMA scheme works in an optimal fashion.

There are, however, many other cases where a cellular infrastructure is not physically available, as in battlefields or temporary work sites where a wireless link between team members is required. For such systems, the “net” concept can be applied, where a set of users (called the “net”) is assigned with a unique PN code sequence. All users in the net have a common frequency hopping pattern, rather than having a unique pattern for each user. All handsets in the net can hear on-going conversations; however, there is only one complete bi-directional communication link between handsets (master/slave) at a given time. In this scenario, the first handset powered on in the net (usually the team leader) becomes the master and provides a frame reference to all other users. The next handset becomes the slave and can communicate with the master. When the master ceases to transmit,
the slave will automatically become the master. Other users in the net can use the transmit link only when one of the two active users stop transmitting. Figure 6-31(b) shows this multi-user scenario.
Chapter 7

Conclusions

This research has been focused on the system trade-offs, hardware architecture definition, baseband processing block design, and synchronization algorithm development of a frequency-hopped transceiver for wireless personal communications. Robust operation of the transceiver is achieved through the use of space diversity (dual antennas with equal gain combining), frequency diversity (frequency-hopped spread spectrum), and time diversity (sequential hop combining and channel coding with interleaving). The proposed transceiver employs novel architectural techniques, such as digital hopping frequency synthesis, direct conversion, SSB modulation, hard-limiting, and multiplierless quaternary FSK detection.

The digital frequency synthesis technique enables the fast hopping required
for an FH-CDMA system and makes FSK signalling easier. The TDD scheme allows one hopping synthesizer to be shared between transmit and receive modes. The hop rate has been chosen to minimize the channel filter’s transient distortions. The DC-offset problem frequently encountered in direct-conversion transceivers can be easily dealt in an FSK system without resorting to expensive signal processing. The SSB modulation technique eliminates often difficult-to-implement image-reject filters for signal upconversion, permits the DDFS to operate over half the hopping bandwidth, and generates accurate I-Q signals for quadrature downconversion. A baseband multiplierless correlation detector has been proposed to detect hard-limited FSK signals without automatic gain control at RF.

These techniques combined allow a highly integrated monolithic solution of the entire transceiver, thus achieving the low power and low complexity required for a handheld communications device without sacrificing performance. Robust synchronization algorithms and blocks, which include RSSI-aided acquisition, pattern matching logic of a 21-digit Barker code, and digital PLL-based frequency and time tracking loops, have been also developed. The transceiver specifications are summarized in Table 7-1.

In order to validate the proposed design techniques, a prototype handset using a monolithic CMOS transceiver [69] in addition to control logic and data interface implemented in a field programmable gate array (FPGA) is being developed by a team of researchers. The first prototype will demonstrate a point-to-
point simplex communication link in the 902-928 MHz ISM band to support 32 kbps voice and (channel) data rates up to 160 kbps. The techniques, algorithms, and analysis developed in this research can be easily adapted and modified to target a wide variety of emerging wireless applications.

<table>
<thead>
<tr>
<th>Multiple Access Scheme</th>
<th>Frequency-Hopped CDMA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation Scheme</td>
<td>Quaternary/Binary FSK</td>
</tr>
<tr>
<td>Duplexing Mode</td>
<td>Time-Division Duplex</td>
</tr>
<tr>
<td>Channel Coding</td>
<td>Convolutional Code (R=1/2, K=6)</td>
</tr>
<tr>
<td>Hopping Bandwidth</td>
<td>26 MHz (902-928 MHz)</td>
</tr>
<tr>
<td>Data Rates</td>
<td>2 - 160 kbit/s</td>
</tr>
<tr>
<td>Frequency Hop Rate</td>
<td>1 hop per 8 symbols</td>
</tr>
<tr>
<td>Antenna Diversity</td>
<td>2 with separate Rx channels</td>
</tr>
<tr>
<td>Maximum Range</td>
<td>500 meters</td>
</tr>
<tr>
<td>Transmission Power</td>
<td>20 μW - 20 mW</td>
</tr>
</tbody>
</table>

Table 7-1  FH/SS Transceiver Specifications
# Appendix A

## Digital Wireless Standards

<table>
<thead>
<tr>
<th>System</th>
<th>CT2</th>
<th>DECT</th>
<th>GSM</th>
<th>IS-54</th>
<th>IS-95</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application</td>
<td>Cordless</td>
<td>Microcellular</td>
<td>Cellular</td>
<td>Cellular</td>
<td>Cellular</td>
</tr>
<tr>
<td>Modulation</td>
<td>GFSK</td>
<td>GFSK</td>
<td>GMSK</td>
<td>π/4-DQPSK</td>
<td>BPSK/QPSK</td>
</tr>
<tr>
<td>Detection</td>
<td>Noncoherent</td>
<td>Noncoherent</td>
<td>Coherent</td>
<td>Coherent</td>
<td>Coherent</td>
</tr>
<tr>
<td>Forward Band (MHz)</td>
<td>864-868</td>
<td>1880-1900</td>
<td>935-960</td>
<td>869-894</td>
<td>869-894</td>
</tr>
<tr>
<td>Reverse Band (MHz)</td>
<td>864-868</td>
<td>1880-1900</td>
<td>890-915</td>
<td>824-849</td>
<td>824-849</td>
</tr>
<tr>
<td>Multiple Access</td>
<td>FDMA/TDD</td>
<td>TDMA/TDD</td>
<td>TDMAFDD</td>
<td>TDM/FDD</td>
<td>CDMA/FDD</td>
</tr>
<tr>
<td>Carrier Spacing (kHz)</td>
<td>100</td>
<td>1728</td>
<td>200</td>
<td>30</td>
<td>1250</td>
</tr>
<tr>
<td>Channels/Carrier</td>
<td>1</td>
<td>12</td>
<td>8</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>Bw/2-way Ch (kHz)</td>
<td>100</td>
<td>144</td>
<td>50</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>Modulation Rate (kb/s)</td>
<td>72</td>
<td>1152</td>
<td>271</td>
<td>48.6</td>
<td>1228.8 (chip rate)</td>
</tr>
<tr>
<td>Speech Codec (kb/s)</td>
<td>ADPCM (32)</td>
<td>ADPCM (32)</td>
<td>RPE-LTP (13)</td>
<td>VSELP (8)</td>
<td>QCCEL (1-8)</td>
</tr>
<tr>
<td>Channel Coding</td>
<td>None</td>
<td>CRC</td>
<td>Conv. R=1/2</td>
<td>Conv. R=1/2</td>
<td>Conv. R=1/2, 1/3</td>
</tr>
<tr>
<td>Portable Tx Power: Peak/Avg (W)</td>
<td>0.01/0.005</td>
<td>0.25/0.01</td>
<td>2-20/0.25-2.5</td>
<td>3/0.6</td>
<td>3/0.6</td>
</tr>
</tbody>
</table>
Appendix B

Glossary

ADC  Analog-to-digital converter
ADPCM  Adaptive differential pulse code modulation
AGC  Automatic gain control
AMPS  Advanced Mobile Phone Service
AWGN  Additive white Gaussian noise
BB  Baseband
BER  Bit error rate
BPF  Band-pass filter
BPSK  Binary phase-shift keying
CDMA  Code-division multiple access
CELP  Codebook excited linear prediction (speech coding)
CMOS  Complementary Metal Oxide Silicon (technology)
CPFSK  Continuous-phase frequency-shift keying
CPM  Continuous phase modulation
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC</td>
<td>Cyclic redundancy check</td>
</tr>
<tr>
<td>CT2</td>
<td>Cordless Telephone 2 (interim ETSI standard)</td>
</tr>
<tr>
<td>CV</td>
<td>Correlation value</td>
</tr>
<tr>
<td>CVSD</td>
<td>Continuously variable slope delta (modulator)</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-analog converter</td>
</tr>
<tr>
<td>DCO</td>
<td>Digitally-controlled oscillator</td>
</tr>
<tr>
<td>DDFS</td>
<td>Direct digital frequency synthesizer</td>
</tr>
<tr>
<td>DECT</td>
<td>Digital European Cordless Telecommunications</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay-locked loop</td>
</tr>
<tr>
<td>DPLL</td>
<td>Digital phase-locked loop</td>
</tr>
<tr>
<td>DPSK</td>
<td>Differential phase-shift keying</td>
</tr>
<tr>
<td>DQPSK</td>
<td>Differential quaternary phase-shift keying</td>
</tr>
<tr>
<td>DS</td>
<td>Direct sequence (spread spectrum technique)</td>
</tr>
<tr>
<td>EIA</td>
<td>Electronic Industries Association (U.S.)</td>
</tr>
<tr>
<td>ETSI</td>
<td>European Telecommunications Standard Institute</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commission (U.S.)</td>
</tr>
<tr>
<td>FD</td>
<td>Frequency detector</td>
</tr>
<tr>
<td>FDD</td>
<td>Frequency-division duplexing</td>
</tr>
<tr>
<td>FDMA</td>
<td>Frequency-division multiple access</td>
</tr>
<tr>
<td>FFH</td>
<td>Fast frequency hopping</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier transform</td>
</tr>
<tr>
<td>FH</td>
<td>Frequency hopping (spread spectrum technique)</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite impulse response (filter)</td>
</tr>
<tr>
<td>FLL</td>
<td>Frequency-locked loop</td>
</tr>
<tr>
<td>FM</td>
<td>Frequency modulation</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
</tr>
<tr>
<td>---------</td>
<td>------------</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field programmable gate array</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency-shift keying</td>
</tr>
<tr>
<td>FTL</td>
<td>Frequency tracking loop</td>
</tr>
<tr>
<td>GFSK</td>
<td>Gaussian filtered FSK</td>
</tr>
<tr>
<td>GMSK</td>
<td>Gaussian minimum-shift keying</td>
</tr>
<tr>
<td>HD</td>
<td>Hard decision</td>
</tr>
<tr>
<td>HPF</td>
<td>High-pass filter</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite impulse response (filter)</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communication (ETSI, Europe)</td>
</tr>
<tr>
<td>IS-54</td>
<td>Interim Standard 54 (TIA/EIA TDMA cellular standard, U.S)</td>
</tr>
<tr>
<td>IS-95</td>
<td>Interim Standard 95 (TIA/EIA CDMA cellular standard, U.S.)</td>
</tr>
<tr>
<td>ISDN</td>
<td>Integrated Services Digital Network</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial, Scientific, and Medical (bands, devices)</td>
</tr>
<tr>
<td>LO</td>
<td>Local oscillator</td>
</tr>
<tr>
<td>LOS</td>
<td>Line of sight</td>
</tr>
<tr>
<td>LP</td>
<td>Loop filter</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-pass filter</td>
</tr>
<tr>
<td>LSB</td>
<td>Least significant bit</td>
</tr>
<tr>
<td>NC</td>
<td>Noncoherent</td>
</tr>
<tr>
<td>NCO</td>
<td>Numerically-controlled oscillator</td>
</tr>
<tr>
<td>PBX</td>
<td>Private branch exchange</td>
</tr>
<tr>
<td>PCN</td>
<td>Personal Communications Network</td>
</tr>
<tr>
<td>PCS</td>
<td>Personal Communications Services</td>
</tr>
<tr>
<td>PD</td>
<td>Phase detector</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>PG</td>
<td>Processing gain</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked loop</td>
</tr>
<tr>
<td>PN</td>
<td>Pseudo-random noise</td>
</tr>
<tr>
<td>PSK</td>
<td>Phase-shift keying</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature amplitude modulation</td>
</tr>
<tr>
<td>QFSK</td>
<td>Quaternary frequency-shift keying</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RSSI</td>
<td>Receiver signal strength indicator</td>
</tr>
<tr>
<td>SCF</td>
<td>Switched-capacitor filter</td>
</tr>
<tr>
<td>SD</td>
<td>Soft decision</td>
</tr>
<tr>
<td>SFH</td>
<td>Slow frequency hopping</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
</tr>
<tr>
<td>SS</td>
<td>Spread spectrum (technique)</td>
</tr>
<tr>
<td>SSB</td>
<td>Single sideband (modulation)</td>
</tr>
<tr>
<td>TDD</td>
<td>Time-division duplexing</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time-division multiple access</td>
</tr>
<tr>
<td>TIA</td>
<td>Telecommunications Industry Association (U.S.)</td>
</tr>
<tr>
<td>TTL</td>
<td>Time tracking loop</td>
</tr>
<tr>
<td>VC(X)O</td>
<td>Voltage-controlled (crystal) oscillator</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very-large-scale integrated circuit</td>
</tr>
<tr>
<td>VSELP</td>
<td>Vector sum excited linear prediction (speech coding)</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless local area network</td>
</tr>
</tbody>
</table>
Bibliography


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