

Microstrip Filter Design Using Electromagnetics

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Introduction

Electromagnetic field-solvers have given the microwave design engineer new tools to attack his or her more difficult design problems. Besides providing valuable analytical data, the visualization capabilities of these new tools can lead to startling new insights into how microwave components actually behave [1,2]. Perhaps you have had a colleague who could look at microwave structure and "see fields". These rare individuals are highly regarded for their grasp of especially challenging design problems. Those engineers not blessed with this gift can use the visualization tools in today's field-solvers to develop some of these skills and see their design work in an entirely new way.

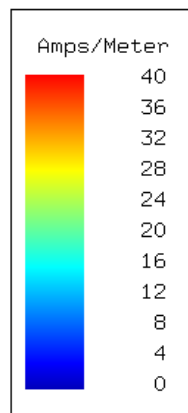
Long solution times limited early users of field-solvers to an analysis of fixed geometries. These solutions are still quite valuable on their own or as sets of solutions that can be used to generate circuit theory based models. With faster computers and more efficient software, it is now possible to optimize some planar microwave circuits using direct driven electromagnetic simulation. Although practical problem size is still limited, field-solver tools can now be more fully integrated into the design environment.

In this talk we will start with some simple microstrip geometries to introduce basic field-solver and visualization concepts. Next, the field-solver will be used to analyze several microstrip discontinuity problems of general interest. Finally, a number of filter design case histories will demonstrate how a designer might apply the analytical and visualization capabilities of these tools to real world problems.

Outline

- A. Introduction to the field-solver and a new way of "seeing".
 - 1. Standing waves on a mismatched transmission line.
 - 2. Microstrip short circuit.
 - 3. Microstrip open circuit.
 - 4. Thin-film termination.
- B. A look at some microstrip discontinuities.
 - 1. Via holes and slots.
 - 2. Mitered bend.
 - 3. Tee-junction.
- C. Applying the field-solver to microstrip filter design.
 - 1. Interdigital bandpass filters.
 - 2. Parallel-coupled-resonator 22.5 GHz bandstop filter.
 - 3. Pseudo-lumped 22.5 GHz bandpass filter.
 - 4. Pseudo-lumped 3.72 GHz bandpass filter.

A note on the color plots:



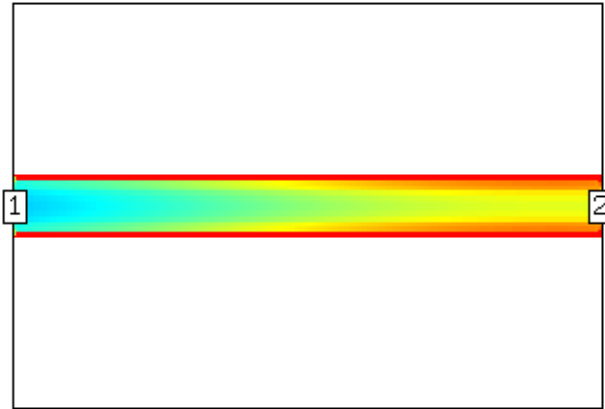
The most desirable method of presentation would include a scale for each color plot. Unfortunately, time and space do not permit this. In all cases red will indicate high values and dark blue will indicate low values. The scale will be stated in the text whenever possible.

Standing Waves on a 50 Ohm Line

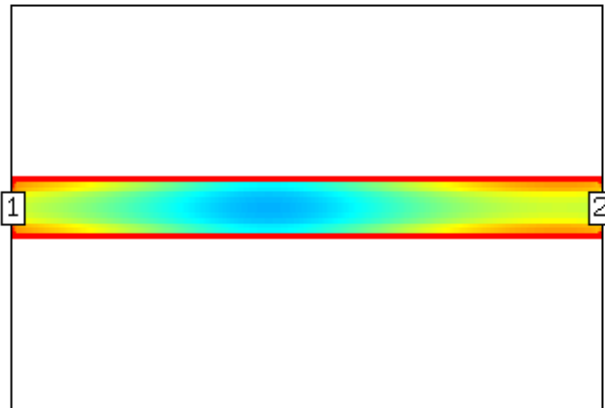
Let's start our introduction to the field-solver with a simple 50 ohm line. The line is 24 mil wide and 225 mil long on a 25 mil thick alumina substrate. There is a generator at port one and a 25 ohm termination at port two, so we expect to see some kind of standing wave [3].



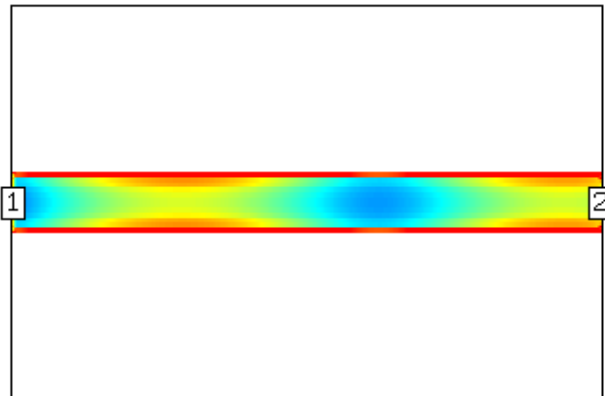
This is the conduction current density on the line at 5 GHz. At this frequency the line is roughly 90 degrees long. There is a clear maximum at the right and a minimum on the left. We are plotting the vector magnitude of the X and Y directed currents.

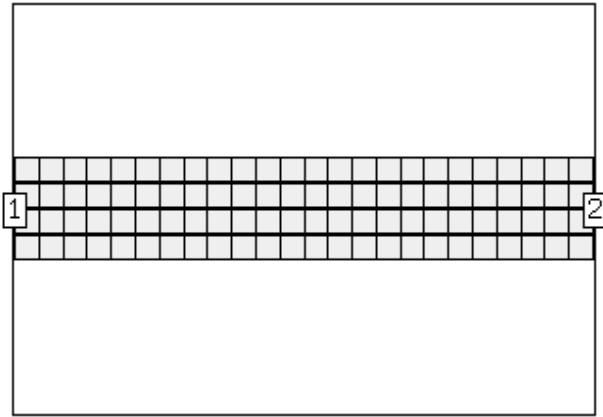


This current plot is at 10 GHz where the line is nearly 180 degrees long.

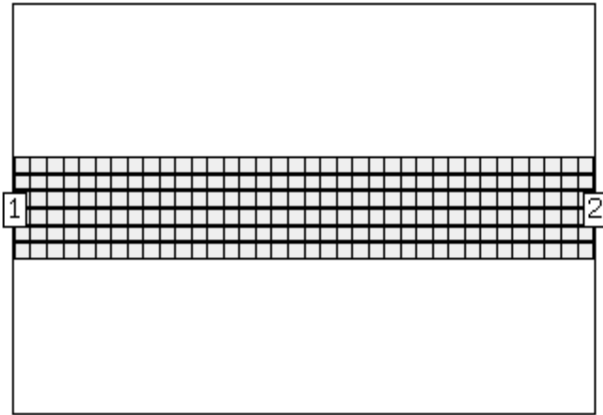


At 15 GHz the standing wave pattern is quite evident. In all three plots we can also observe how the current maximizes on the edges of the strip. Why doesn't the current go to zero on the edges of the strip at the current minima? Complete cancellation does not occur at the minima because the forward and reverse waves do not have the same amplitude.

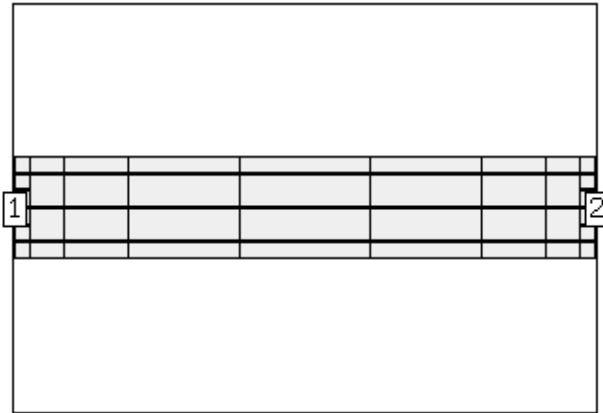




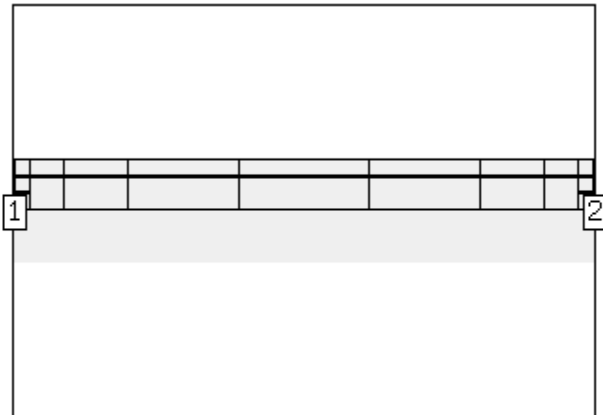
This is all very interesting but how did the software generate these current density plots? This particular code [4,5] uses the method of moments to solve for the currents on the planar conductors. Here the 50 ohm line is divided into "cells" that are 6 mil on a side. The software solves for X and Y directed currents on each cell.



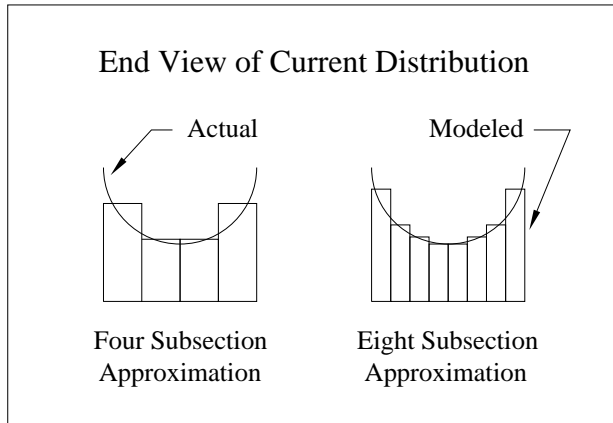
To get more accuracy we can use smaller cells to approximate the actual current distribution. Here the cells are 4 mil on a side. Unfortunately, solution time increases very rapidly as we increase the number of cells. If we have N cells then eventually we must invert an N by N matrix. The solution time is proportional to a factor between N^2 and N^3 .



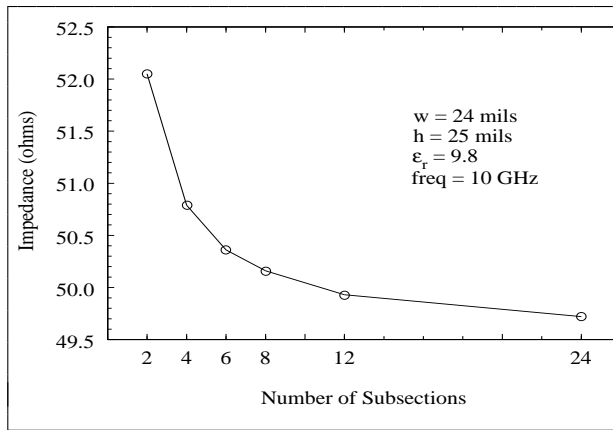
One way to speed up the solution is to combine cells into "subsections". The subsection dimensions must be integer multiples of the cell size. This results in a much smaller matrix to invert. If the subsections are no larger than lambda over 20 at the highest frequency of interest, then we usually have enough accuracy. Here the 50 ohm line has been subsectioned using the lambda over 20 rule at 15 GHz.



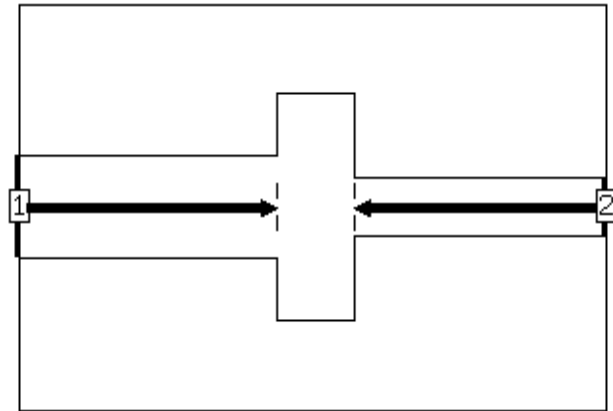
Another way to reduce the solution time is to use symmetry whenever possible. This can literally cut the problem size by two and may decrease the solution time by a factor of 4 to 8. Here we see our 50 ohm line with only the top half subsectioned.



You may have noticed earlier that the currents maximize on the edges of the strip. Why is this? For a low loss line, the charges that make up the current repel and we get the charge/current distribution shown here. To accurately approximate this distribution, we need several subsections across the width of the strip. The computed impedance of the line will converge as we increase the number of subsections across the width.

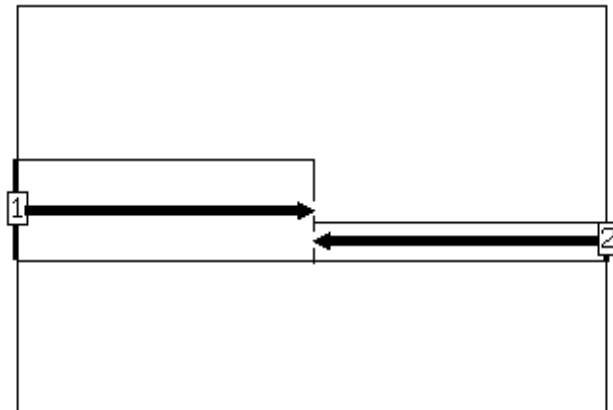


This plot shows how the computed line impedance converges as the number of subsections across the strip increases [6,7]. In one of the design examples we will observe this convergence behavior in a spiral inductor model.

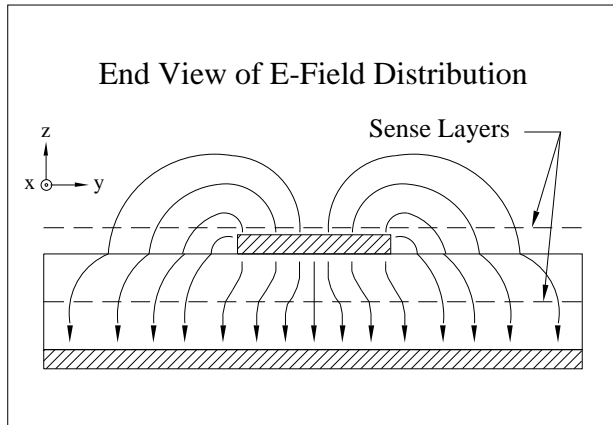


De-embedding

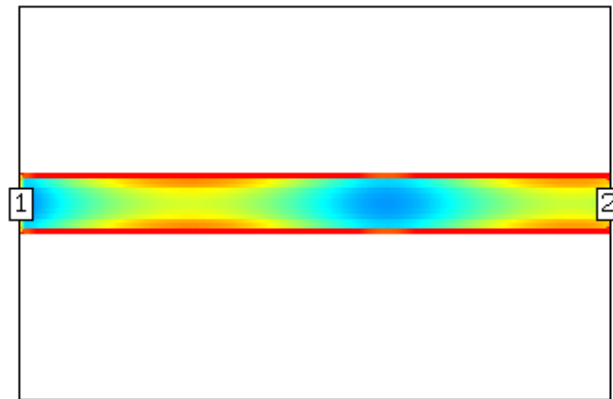
The impedance data above was computed by de-embedding. De-embedding removes a length of line from the overall solution and moves the reference plane used to compute S-parameters. We will use de-embedding on many of the field-solver problems discussed here. The heavy black lines and arrows indicate the location of the new reference planes.



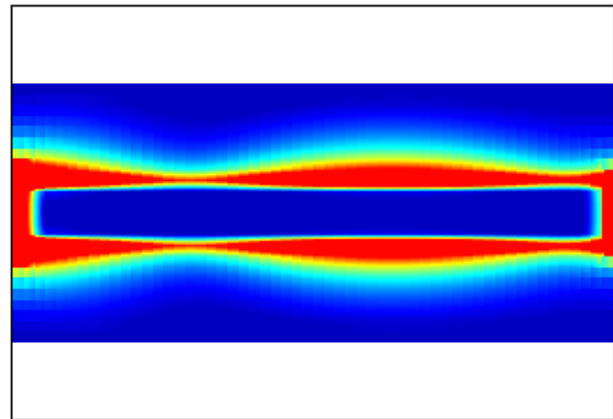
Sometimes the de-embedded network has zero physical length, as in the step discontinuity on the left. Removing the uniform line on both sides captures the characteristics of the step in the resulting two-port data. When this data is used in a simulation, lengths of line with the same electrical parameters are re-attached to the step. The electrical performance of the step is then included in the overall simulation.



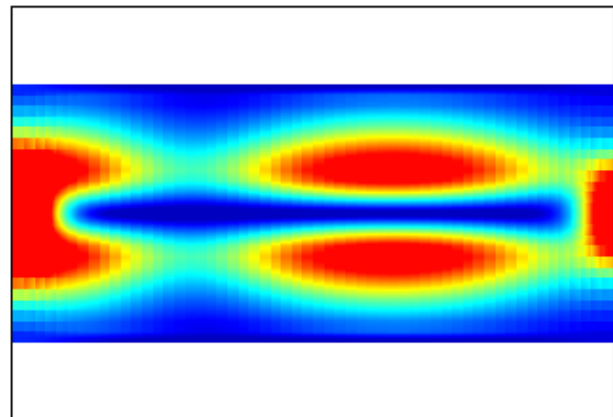
Although this software computes current, we can get an indirect view of the voltage by using a very old trick. A one megohm per square sheet resistor will sense the voltage in an X-Y plane which is proportional to the tangential E-field. This is very similar to the "resistance paper" you may have used in your first year physics lab. Here we have placed sheet resistors in the X-Y plane at two different heights.



For reference, here is the 15 GHz current distribution on the 50 ohm line that we looked at earlier.



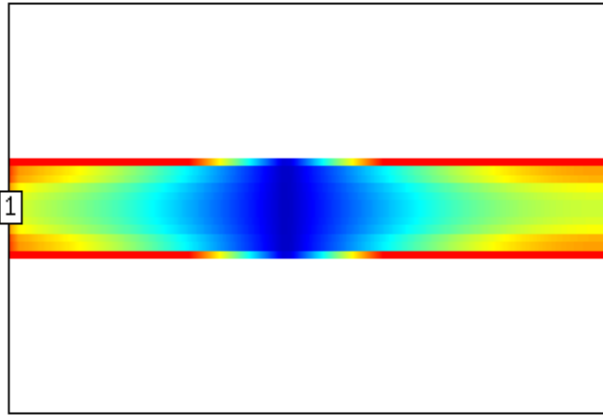
Here the sheet resistor is one mil above the conductor. Note the voltage is 90 degrees out of phase with the current. The voltage scale is 100 - 1000 volts/meter.



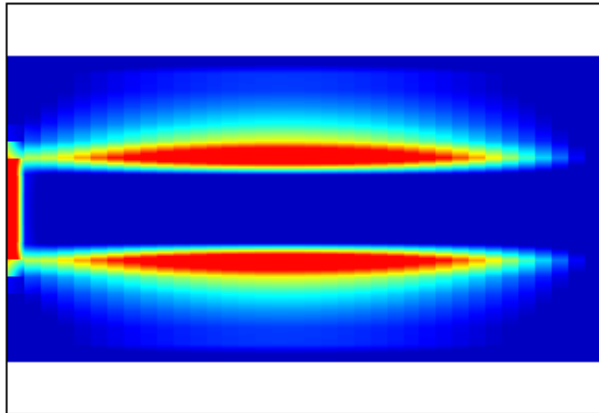
Here the sheet resistor is half way between the strip and the ground plane. Note how far the field extends beyond the edges of the strip. The voltage scale is 30 - 300 volts/meter. Other software packages can display full vector plots of the various field quantities.

Ideal Short Circuit

The second basic structure in our orientation is an ideal short circuit. The generator is at port one and the line terminates in an ideal conductive wall on the right. We expect to see a current maximum at the short circuit. Why doesn't the current spread across the width of the strip? The current follows the shortest path to ground and stays on the edges.

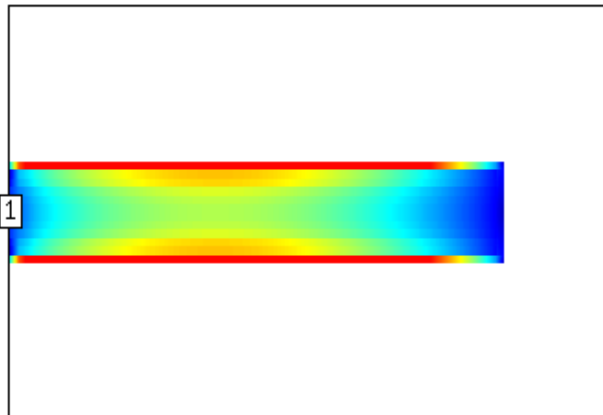


This is the voltage one mil above the line. As we expect, it is 90 degrees out of phase with the current. The voltage scale is 200 - 2000 volts/meter.

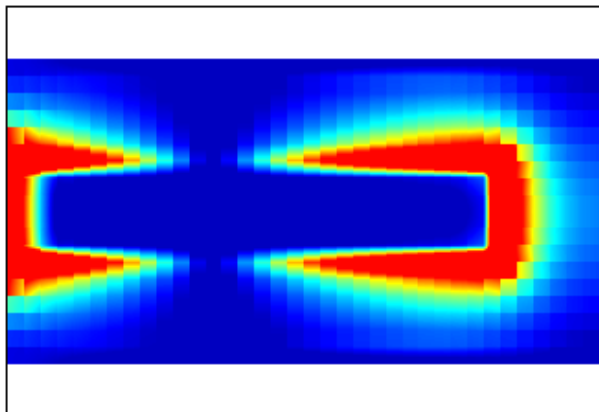


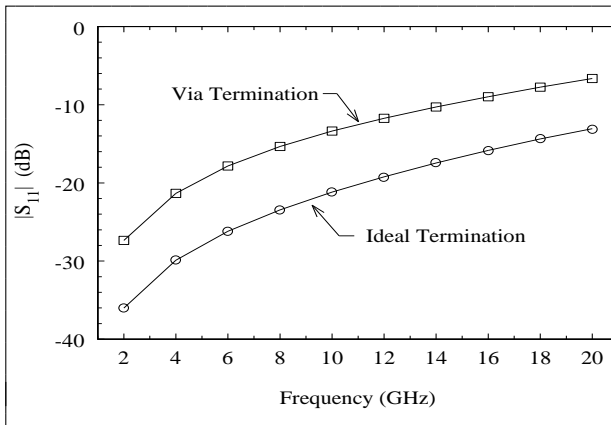
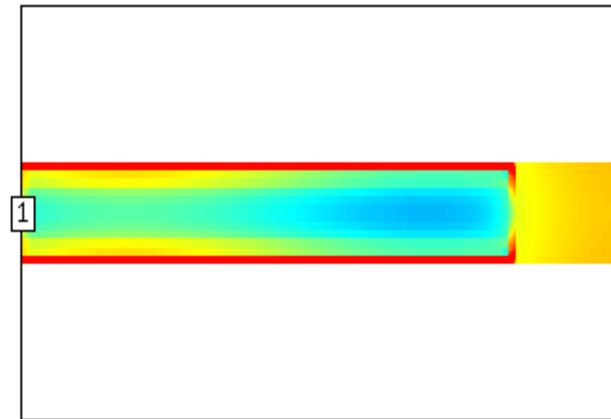
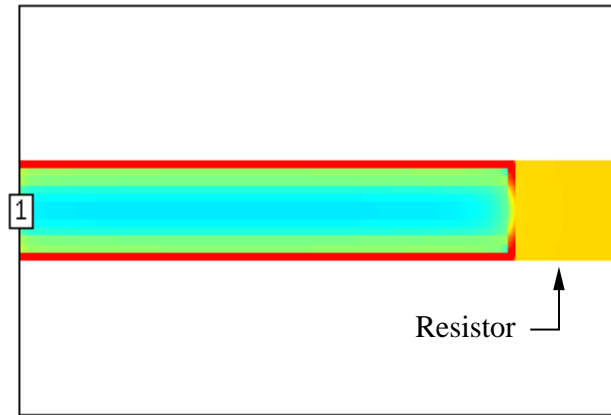
Open Circuit

The next example is a microstrip open circuit. Transmission line theory tells us that the current should be zero and the voltage maximum at the open end.



The voltage one mil above the line maximizes at the open end and is 90 degrees out of phase with the current. The voltage scale is 200 - 2000 volts/meter.



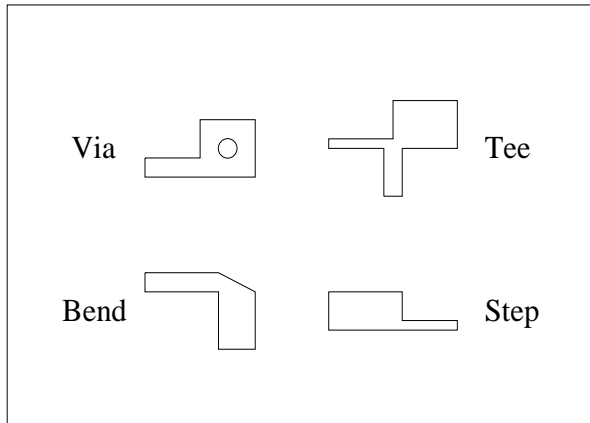


Thin-Film Resistors

Our final example element is a 50 ohm thin-film resistor. A generator is connected to port one and the resistor is terminated by an ideal conductive wall on the right. All the previous microstrip examples might lead us to expect a non-uniform current distribution across the width of the resistor. But at low frequencies (5 GHz) this would violate Ohm's law. The need for uniform current on the resistor also forces a large transverse current on the conductor where it joins the resistor.

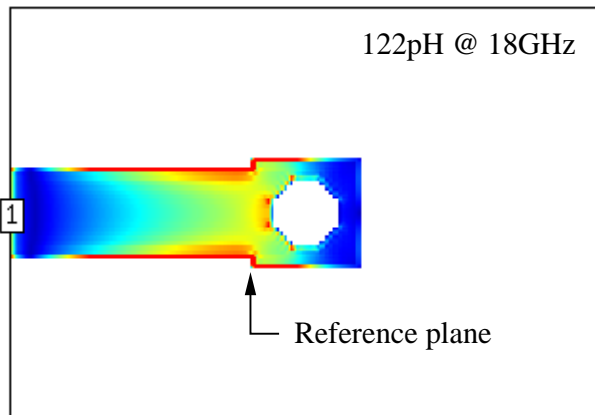
As we go higher in frequency (15 GHz), transmission line theory comes into play. The resistor is getting longer in terms of wavelengths and we do see a finite current distribution across the length of the resistor. In fact, this one plot shows us three fundamental forces in balance. Coulomb's law forces the current to the edges of the conductor. Ohm's law dictates a uniform current density on the resistor. And the wave equation tells us the current must vary sinusoidally along the length of the line. The scale in both plots is 5 - 20 amps/meter.

Our resistor is small, 24 by 24 mil, and its return loss is better than -20 dB up to 10 GHz. But in most circuits our ideal wall is more likely a via hole. The additional inductance of the via seriously degrades the return loss. An interesting exercise would be to compensate the resistor/via combination for better return loss.



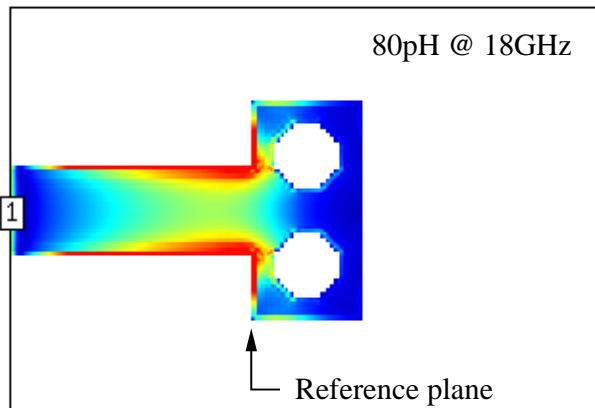
Microstrip Discontinuities

A discontinuity is probably the ideal size problem for today's field-solvers. The average discontinuity problem will solve in, at most, a few minutes per frequency point and data points are only needed every few GHz. The user can easily replace an existing analytical model with computed S-parameters. Or, a more complex network that includes several discontinuities in close proximity might be computed.

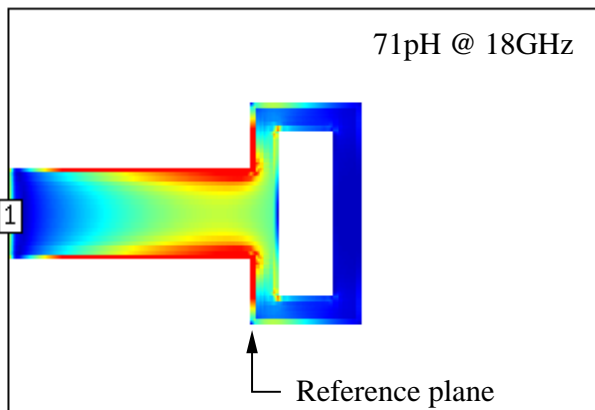


Microstrip Vias and Slots

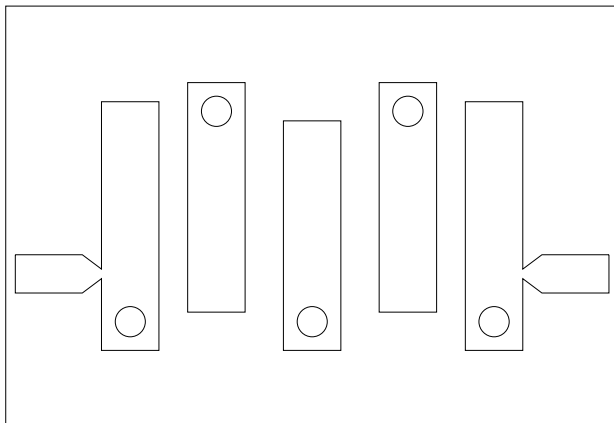
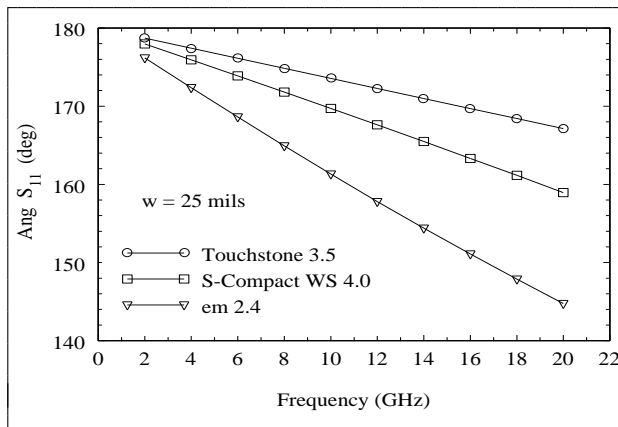
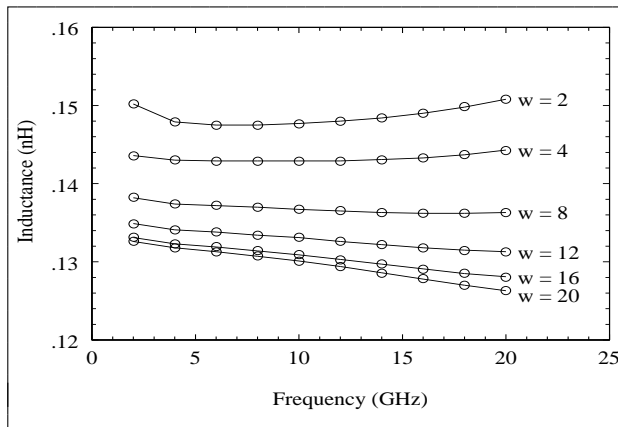
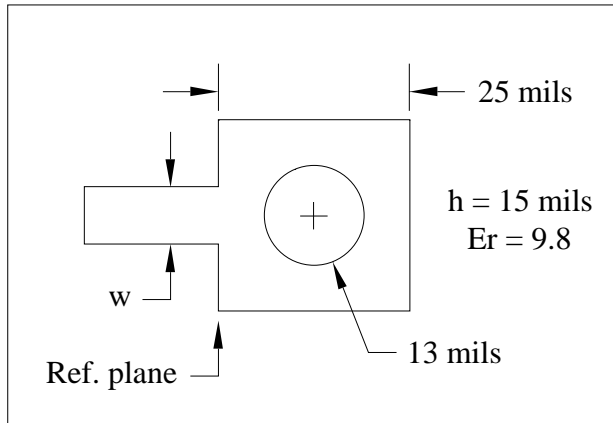
Here is the current distribution on a single microstrip via at 18 GHz. The via pad is 25 mil square, the hole diameter is 13 mil, and the substrate is 15 mil thick. The equivalent inductance at the reference plane is 121.6 pH at 18 GHz. Note that the model includes the via, the surrounding pad, and a step discontinuity. Also note how the current follows the shortest path to ground and uses only one side of the via.



We can lower the inductance by placing a via on each side of the line. The equivalent inductance for this case is 79.6 pH, a decrease of 35% over the single via case. There is probably some mutual inductance between the two vias.



Slots have often been proposed as the lowest inductance alternative. Here we see that the current distribution is very similar to the double via. The inductance is 70.6 pH at 18 GHz, only a marginal improvement over the double via. The current scale is 0 - 40 amps/meter in all three color plots.



The microstrip via is a good example of how a typical user might generate a custom model [8]. In many companies the thin-film fabrication area sets the minimum diameter and pad dimensions of the via. For a given project the substrate thickness and relative dielectric constant are also fixed. The only variable left to the user is the width of the line feeding the pad.

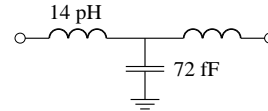
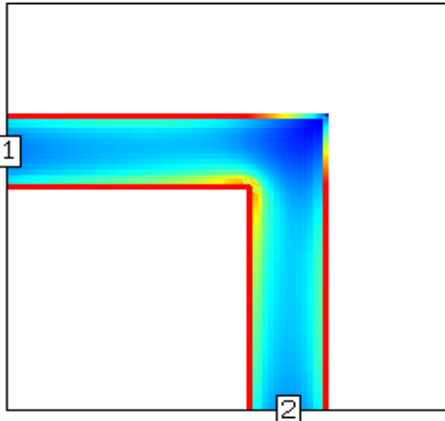
Using batch processing it is easy to solve several via problems as a function of frequency and line width. If Z-parameters are specified, inductance can be computed with a pocket calculator. A designer equipped with several of these plots may not return to the field-solver for new data for many months.

Here the field-solver data for a single via is compared with the analytical models [9,10] available in commercial linear simulators. Why are the analytical models so poor? Perhaps because they start with a uniform current distribution assumption. The exact location of the reference plane and the geometry of the via pad also have a large impact on the computed inductance.

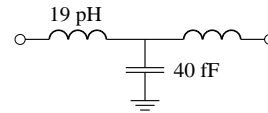
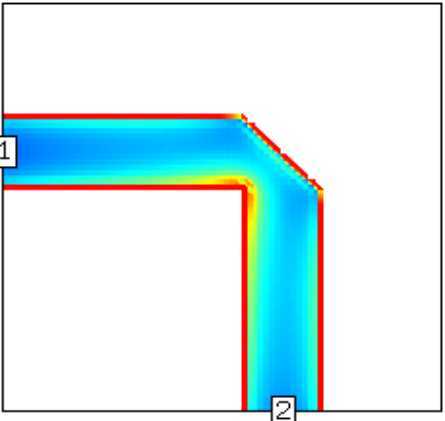
The microstrip interdigital filter is an example we will examine later where the correct via inductance is critical. Errors of a degree or two will seriously compromise the design. The field-solver can also be used to design better grounded mounting pads for MMIC chips [11].

Microstrip Mitered Bend

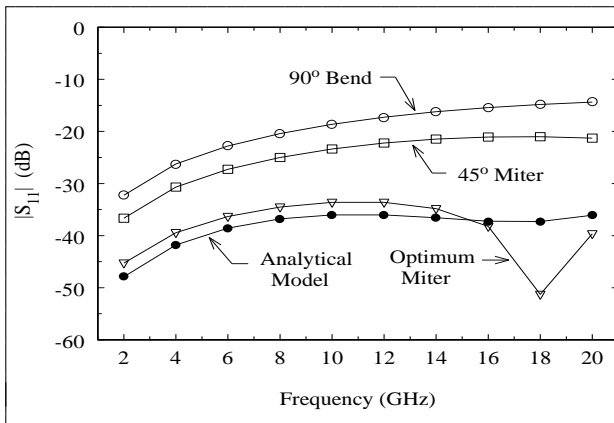
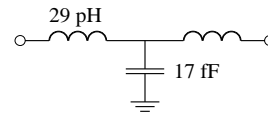
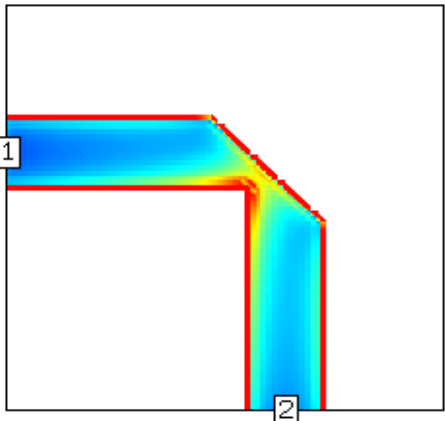
The microstrip bend is a discontinuity where current flow around a corner is critical. On the left is an unmitered bend in a 15 mil wide line on 15 mil alumina. Note the current null at the outer corner and the current maximum on the inner corner.



Here the bend has been mitered with a simple 45 degree cut. The equivalent capacitance has decreased almost 50% and the series inductance has increased slightly.



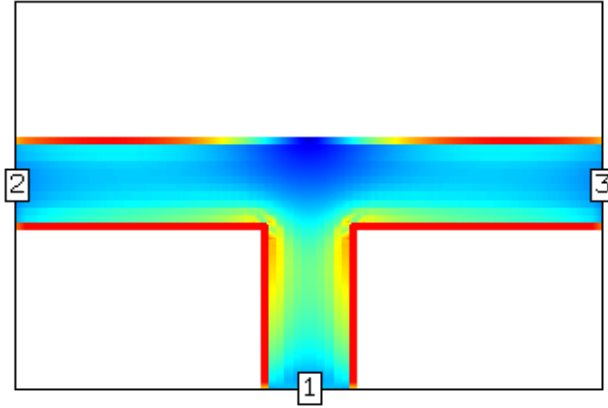
Finally, the "optimum" miter has been computed using a well known formula [12]. The capacitance has been cut in half again and inductance is 2 times larger than the unmitered case. The reference planes for all three lumped models were set to the inside corner. The current scale is 5 - 55 amps/meter in all three color plots.



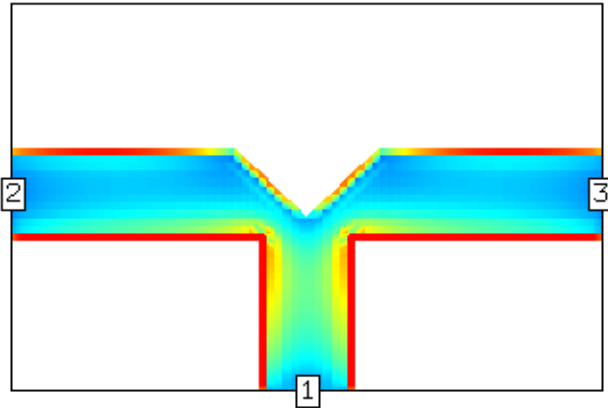
The return loss for all three bends is shown here. Mitering clearly improves the return loss. The analytical model for the optimum miter is also shown. This analytical model seems to work quite well for these substrate parameters and line width. Some recent experimental data on the microstrip bend can be found in Reference 13.

Microstrip Tee-Junction

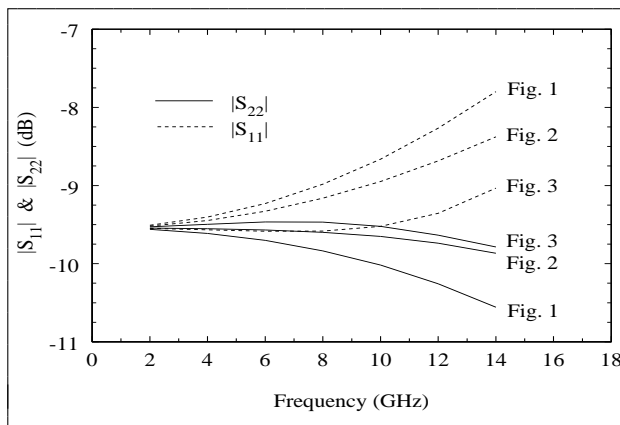
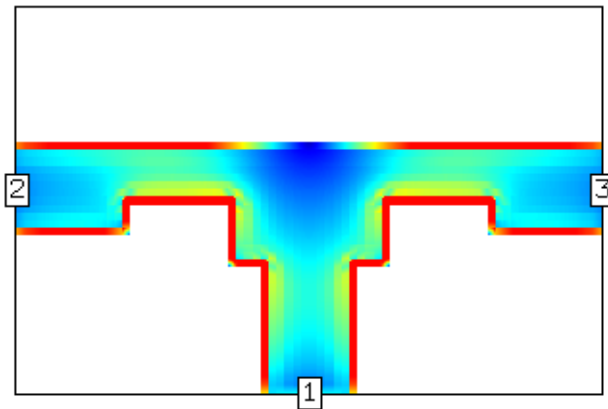
Another interesting and frustrating discontinuity is the tee-junction. The example on the left is driven at port one. Note how the current flows around the corners. It takes considerable time/distance for the normal microstrip current distribution to be re-established on the left and right arms. The result is a considerable area with very little current flow across from the common arm.



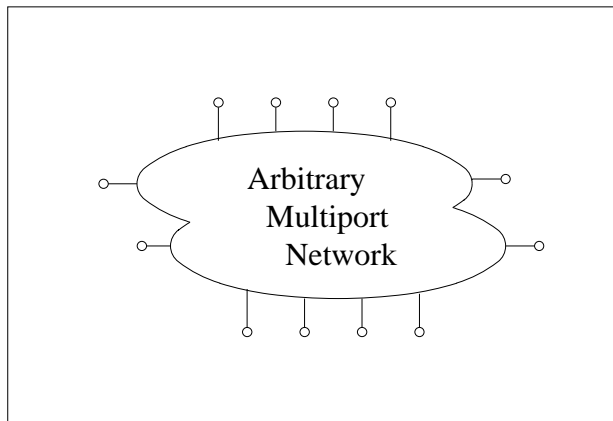
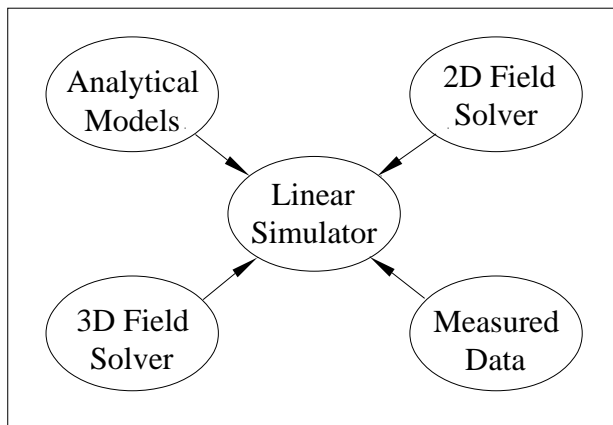
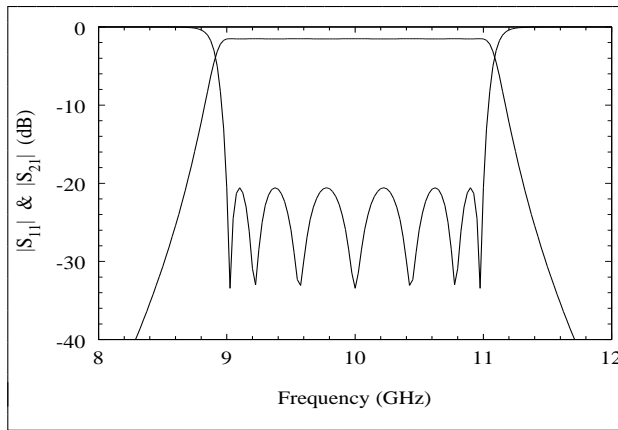
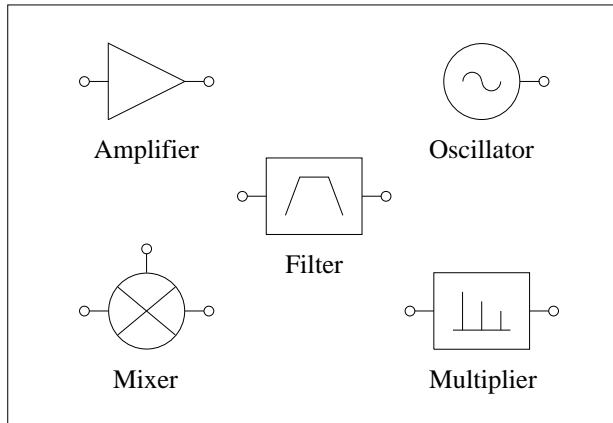
The junction above is unmatched. One published matching technique [14] shapes the "dead" area across from the common arm. The amount of compensation shown here is greater than what was recommended in [14]. This tee was optimized manually by making several runs at 12 GHz and using the mitered bend as a guide.



Another matching technique [15] modifies the common arm and the transition region around the corners. The current scale in all three plots is 0 - 30 amps/meter.



Here is the S-parameter data for the three junctions shown above. The theoretical best match for this three port is -9.5 dB return loss. The second compensation technique appears to be working a little better. Both of these are candidates for optimization on the field-solver using software we will discuss a little later.



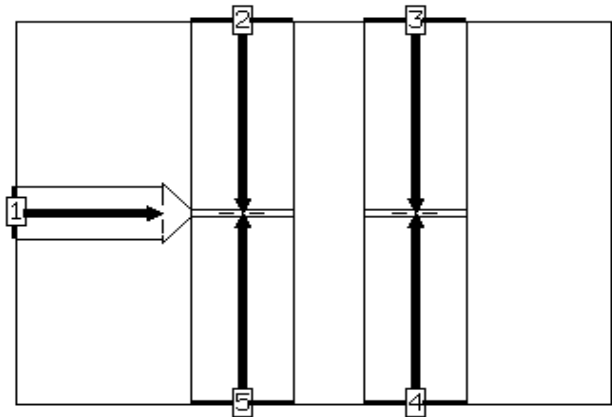
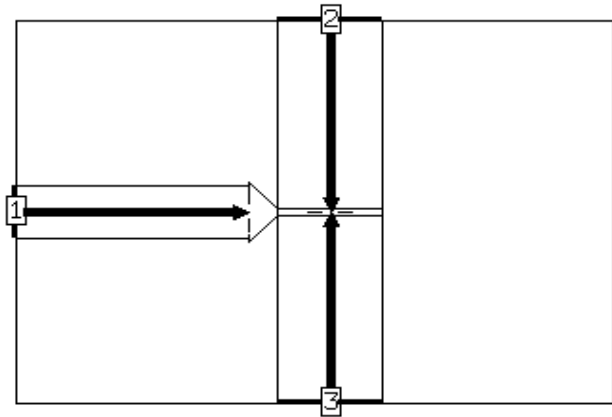
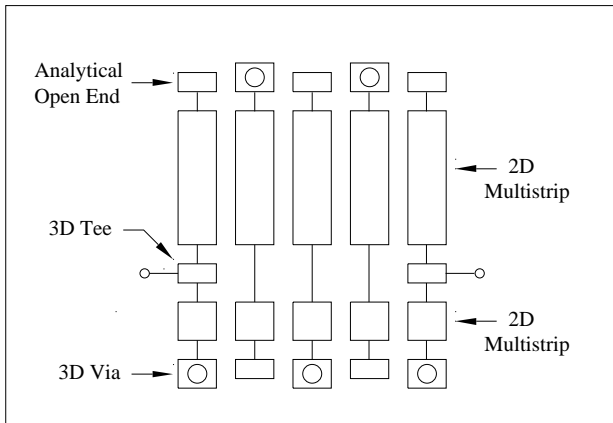
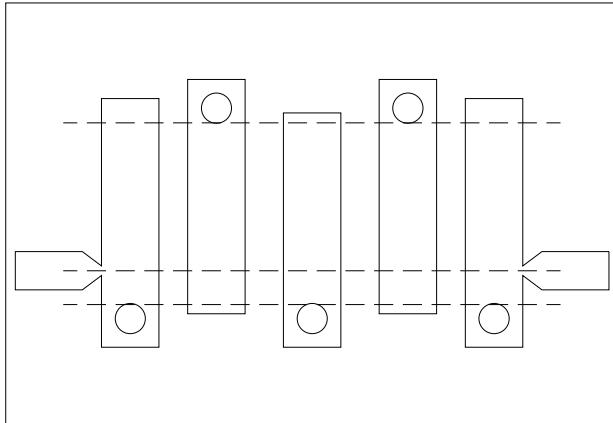
Microstrip Filter Design

A field-solver might help the designer of any microstrip component. When laying out an amplifier, oscillator, mixer, or filter we can often identify regions not easily described using standard library models. In this talk we will focus on filter design.

A filter is a good vehicle to test the usefulness of the field-solver. With a filter there is a well defined, exact answer. It is easy to define error in terms of center frequency shift, bandwidth expansion or contraction, and return loss achieved. The uncertainty in active device parameters make amplifier and oscillator circuits less desirable as test vehicles.

A "hybrid" approach [16,17] using several different types of design tools from several different vendors is often needed to complete a given design task. The tools might include a 3D field-solver, a 2D cross-section-solver, a linear simulator with analytical models, and even measured data. The linear simulator is usually the "glue" that gathers all the data and presents the final analysis. As we will see, optimization using field-solver data is also a possibility.

For this hybrid design approach to be effective, all the available tools must be capable of producing and accepting multiport S-parameter data. It is quite common to generate field-solver results with four to six ports. We have tried some problems with as many as sixteen ports. It is surprising how many design tools still cannot handle anything greater than four port data.



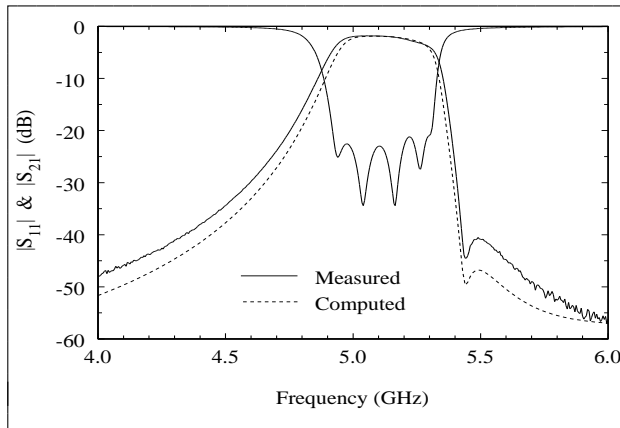
Microstrip Interdigital Filter

The microstrip interdigital filter is very popular with module engineers because of its compact size. The via and tee-junction models discussed earlier are key to modeling this filter correctly. Another key element is a multistrip model which includes all non-adjacent couplings. The dashed lines show how the filter is subdivided for analysis.

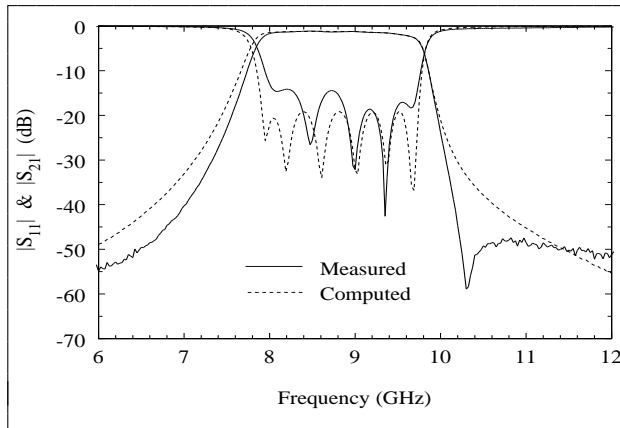
It is not practical to model the complete filter on a 3D field-solver. The most efficient approach is a "hybrid" model using a 2D multistrip model [18,10], 3D discontinuity models, and analytical models all glued together in a linear simulator.

This is the tee-junction configuration currently being used in our interdigital filters. The line connected to port one tapers to the common connection point. Experimentally this seems to work better than a full width common arm. We have not tried any of the compensation techniques discussed earlier. De-embedding to zero length on ports 2 and 3 captures the effects of the non-uniform current distribution for later analysis.

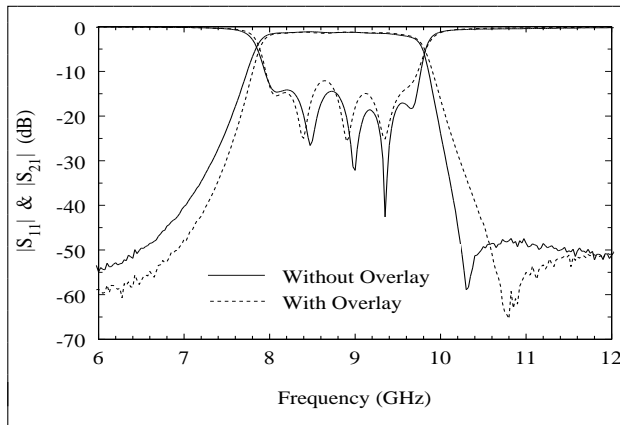
The tee-junction in the filter is not really isolated, there is a second line nearby. De-embedding in the presence of the second line might give us better results. However, I have been unable to try this simple experiment. Touchstone handles multiport data well but does not have the full-wave multistrip model I require. LINMIC+ and Super-Compact have the multistrip model but cannot handle the 5-port data.



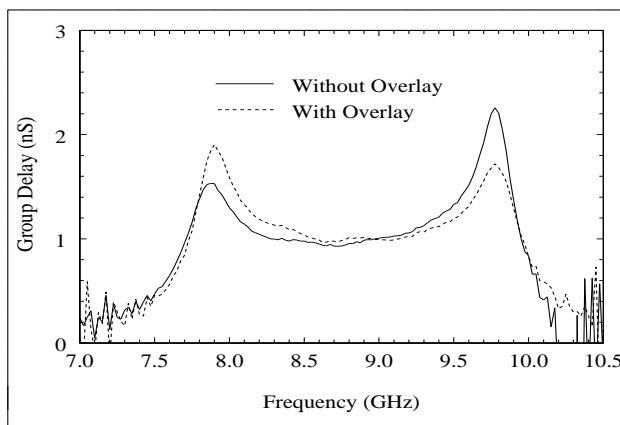
On the left is a tuned, 5th order interdigital filter in C-band. The transmission zero on the high side is caused by the non-adjacent couplings between the strips. The multistrip model is able to predict this zero fairly accurately. The center frequency error is less than 1% and the bandwidth error is 50 MHz or about 9%.



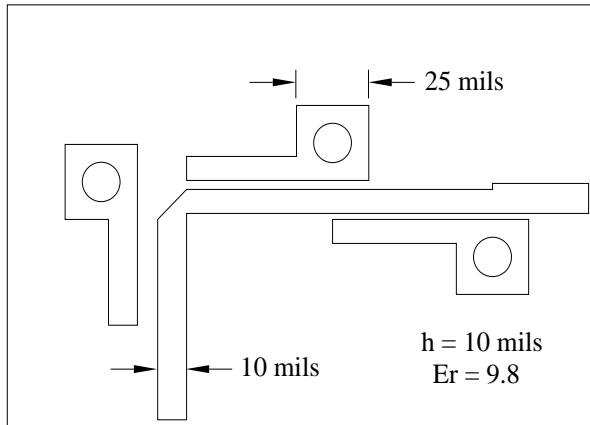
This is an example of a 7th order interdigital filter at turn-on. The substrate is 15 mil thick alumina, $\epsilon_r = 9.8$. At this frequency the multistrip model can no longer predict the location of the transmission zero [19]. A quasi-static multistrip model predicts the transmission zero at all frequencies. But as frequency increases, the quasi-static center frequency prediction will not be accurate. The bandwidth contraction on the low side is caused by evanescent modes and presently cannot be modeled. The bandwidth error is about 70 MHz or 3%.



Adding a dielectric overlay to this same 7th order interdigital filter has some interesting advantages. The most important improvement is in the symmetry of the rejection skirts. The filter with overlay must be re-designed, the gaps between resonators change significantly. The overlay is also 15 mil thick alumina, $\epsilon_r = 9.8$, with no top metal.

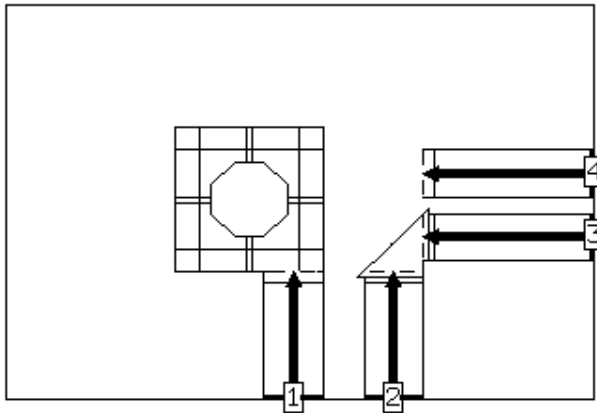


Another advantage of the dielectric overlay is a more symmetrical group delay response. The insertion loss flatness in the passband is also slightly better.

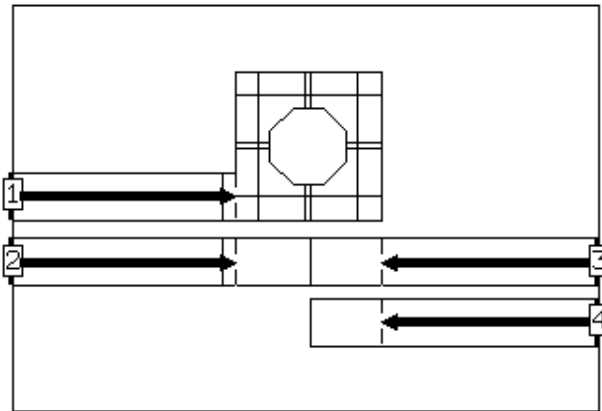


Parallel-Coupled-Resonator 22.5 GHz Bandstop Filter

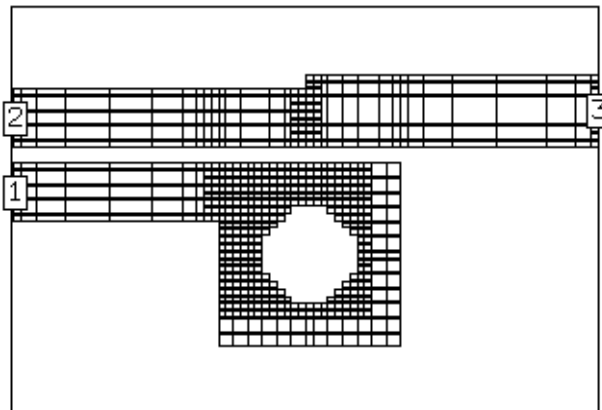
The bandstop filter shown here is a microstrip version of a topology proposed by Schiffman and Matthaei [20]. It is a three resonator filter designed to reject signals from 21.5 GHz to 23.5 GHz and pass signals from 25 GHz to 40 GHz. The layout shown is on 10 mil thick alumina and was designed to fit the I/O locations of an existing substrate. The previous examples would indicate that we need to use the field-solver for at least the via holes.



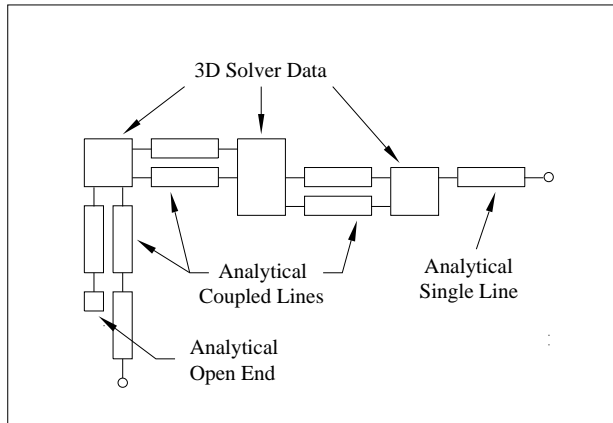
After doing a preliminary layout it became obvious that there are some regions not easily described using a cascade of circuit theory models. The design was subdivided into three multiport field-solver problems connected by analytical coupled line models in a linear simulator. The first field-solver network is centered on the via at the left. Note there are several discontinuities in close proximity: the via and surrounding pad, an asymmetrical step into the via, the mitered bend, and the open end.



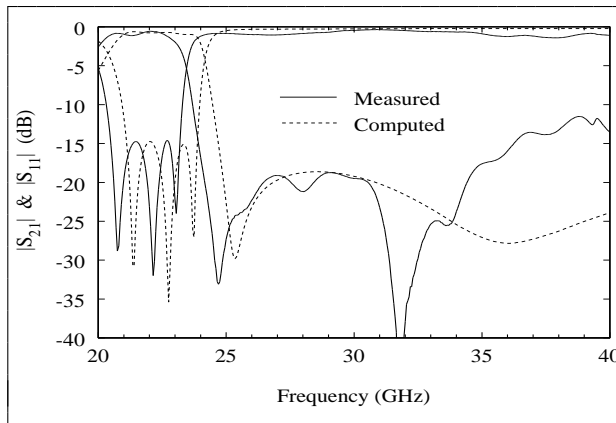
The second field-solver problem tackles the area around the central via. There is an ambiguous region between the second and third resonators due to the size of the via pad. Is the connecting line between the second and third resonators a single line or a coupled line? Where does the second resonator end, at the edge of the pad or the edge of the hole? The outlines show how each network was described to the field-solver to guarantee a good mesh.



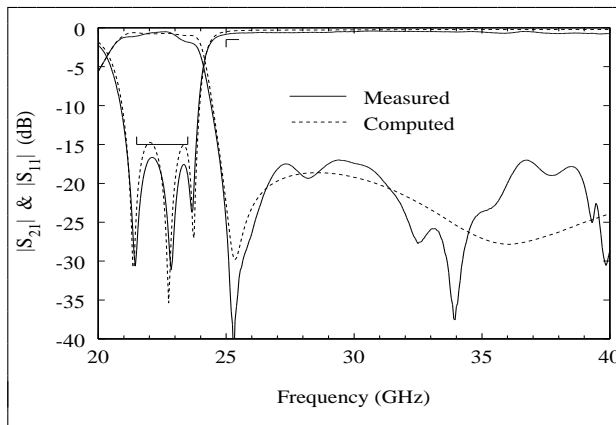
The final field-solver problem concentrates on the via at the far right. Again there is some ambiguity regarding the length of the third resonator depending on how the current terminates on the via hole. Here we have shown the subsectioning of this problem. Using the field-solver on these three networks takes much of the uncertainty out of this design. We can get good analytical data on each network without fully understanding the details of how each one behaves.



This schematic shows how the hybrid solution is built using the field-solver data. An initial estimate of the circuit dimensions is made and a set of field-solver data is computed. The circuit is then optimized; coupled line gaps and line widths are allowed to change. A second set of field-solver data is then computed using the new dimensions and the circuit is optimized again. It is seldom necessary to iterate in this way more than 2 or 3 times.



Here are the measured versus modeled results for the bandstop filter at turn-on. The stopband is shifted about 700 MHz low, almost 3% error at 25 GHz. However, it looks like the bandwidth is correct.



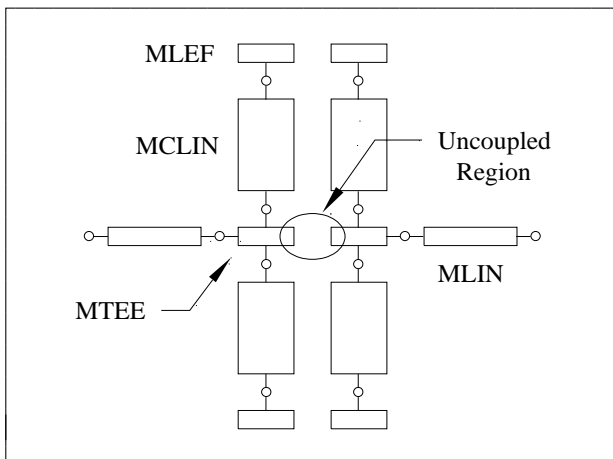
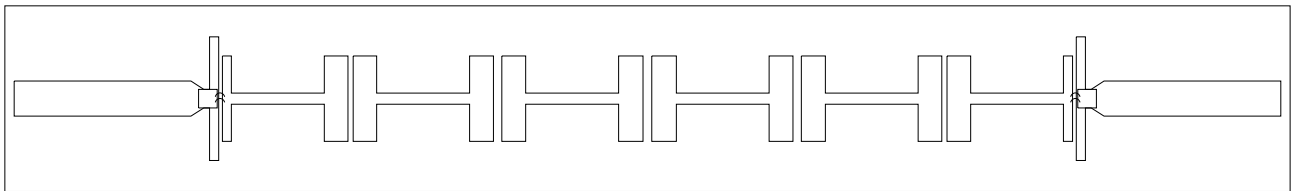
The filter was tuned by scribing off a corner of each resonator at the open-end. The bandwidth is indeed correct which indicates that the gaps are correct. Still, the turn-on response was somewhat disappointing. To determine the source of the error we are examining the via modeling more closely and looking at the manufacturing tolerances.

Pseudo-Lumped 22.5 GHz Bandpass Filter

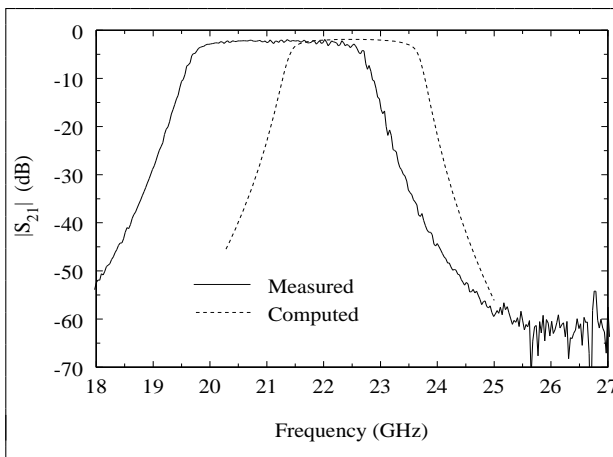
The 22.5 GHz microstrip filter described here is a pseudo-lumped topology fabricated on a thin, low dielectric constant substrate. This topology has been used very successfully at lower microwave frequencies [21,22]; its principle advantage is spurious-free performance out to $4f_0$ or even $5f_0$.

The layout of the bandpass filter is shown below. High impedance transmission lines form series inductors, while pairs of

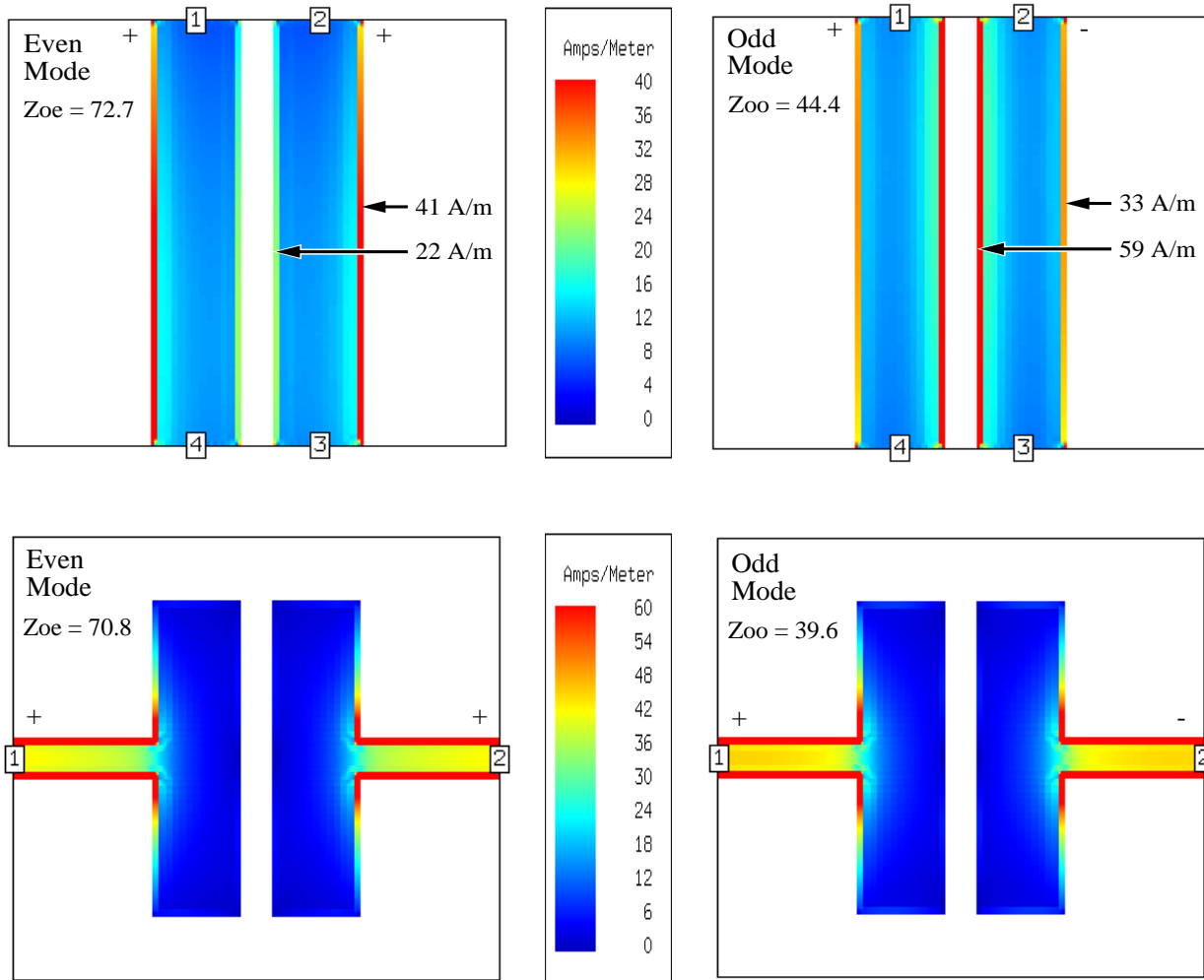
rectangular patches, separated by narrow gaps, form capacitor pi-networks. The substrate material, Trans-Tech D450, is 10 mil thick with a relative dielectric constant of 4.5. The substrate size is 690 mil by 100 mil. The low dielectric constant makes small shunt capacitors realizable and helps prevent higher order modes in the substrate. Parallel plate capacitors are used across the outermost gaps to increase the coupling. A more complete description of this filter can be found in [23].



The first iteration of this filter was designed using the standard microstrip discontinuity models found in any microwave linear simulator. Here is a schematic showing how one of the pi-networks might be modeled. A width of 6 mil was chosen for the series transmission lines. With a 6 mil series line width, the MTEE model introduces an uncoupled region in the center of the pi-network. We expected this uncoupled region to introduce a small, but acceptable, error into the final design. In fact, other errors were far more significant.



Here are the measured versus modeled results for the first iteration filter. The correlation is quite poor between the measured results and the computer model. The center frequency error is 1.31 GHz or 5.8% and the bandwidth error is 830 MHz or 33%.



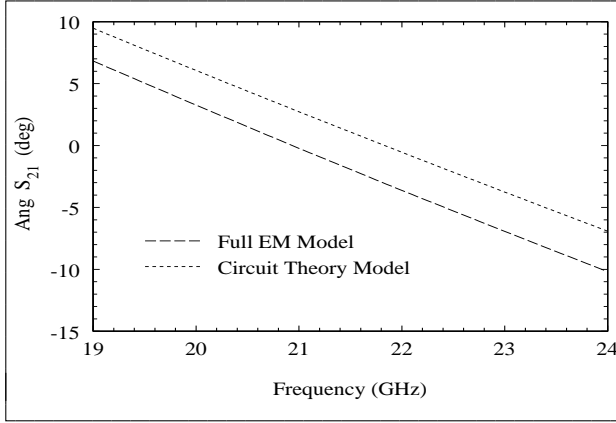
A qualitative interpretation for the behavior of this filter can be found by examining the current distribution on the pi-networks. First let's look at the conventional coupled line case. The top two figures show the even- and odd-mode current distributions on a pair of coupled lines. Ports one and two are the driven ports. In the even-mode, the current is nearly twice as large on the outer edges of the strips compared to the inner edges. The odd-mode case is just the reverse, the current is nearly twice as high on the inner edges of the strips. These current distributions are consistent with the conventional theory for coupled lines.

The bottom two figures display the current distributions on the pi-networks. In the even-mode there is more current on the outer edges of the strips and very little current on the inner edges. The odd-mode current distribution is

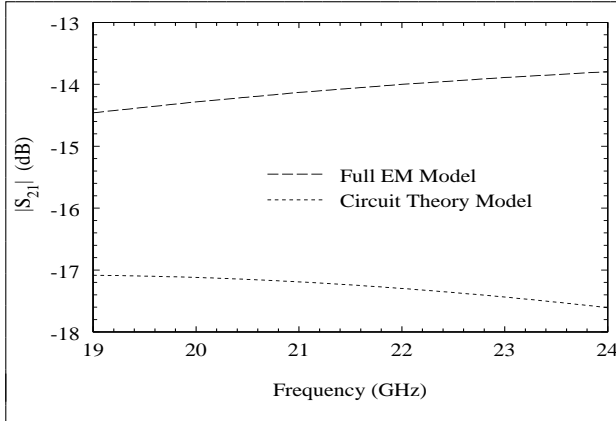
very similar to the even-mode, the current tends to maximize on the outer edges of the strips.

The current distributions on the pi-networks are the key to understanding the large errors in the circuit theory model. Using the conventional model library, we assumed that the pi-network patches could be described by coupled lines with normal even- and odd-mode current distributions. By feeding the pi-networks in the center of the strips, we have forced a current distribution that is quite different from the conventional coupled line case.

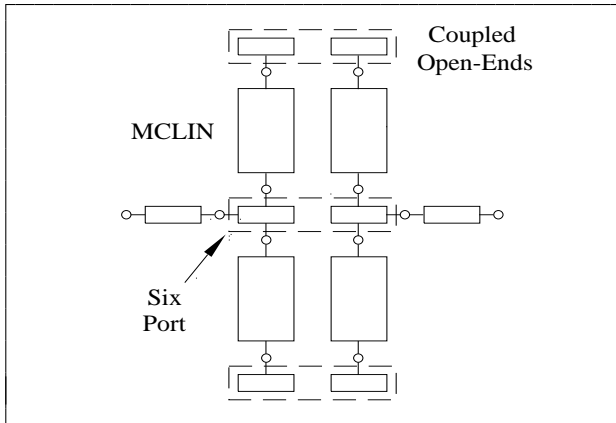
In [23] an even- and odd-mode analysis on the pi-networks concludes that the even-mode impedance is virtually unchanged while the odd-mode impedance is 13% lower than the conventional coupled line case.



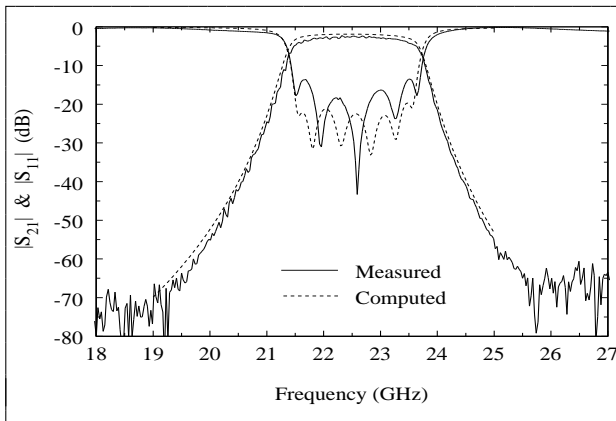
The S_{21} phase angle shows a large difference between the two analysis techniques. At 22.5 GHz the error is 137%. The phase angle error accounts for the center frequency shift in the first iteration filter.



Perhaps the most startling error is in the S_{21} magnitude. This is of course directly related to the change in odd-mode impedance that we noted earlier. The error between the two analysis methods is 3.4 dB or 24% at 22.5 GHz. This accounts for the large bandwidth error in the first iteration filter.



A hybrid approach was again used to model the pi-networks in the second iteration filter. The field-solver was used to generate a six-port model that captures the unconventional current distribution on the pi-networks. The field-solver was also used to generate a coupled open-end model. Coupled line and single line analytical models were used to connect the field-solver solutions.



The turn-on results for the second iteration filter are shown on the left. The pi-network gaps increased by 60% to 80% and the series line lengths decreased by 8% compared to the first iteration filter.

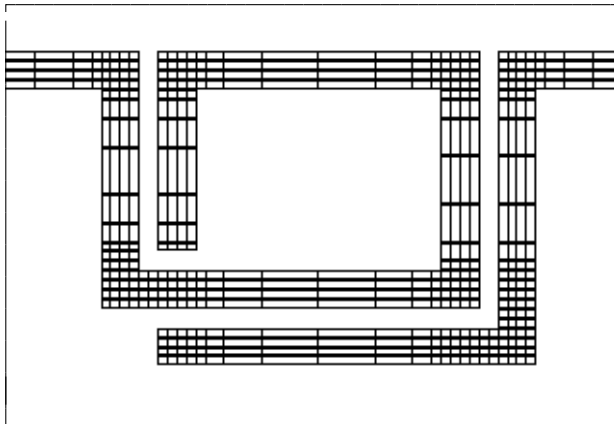
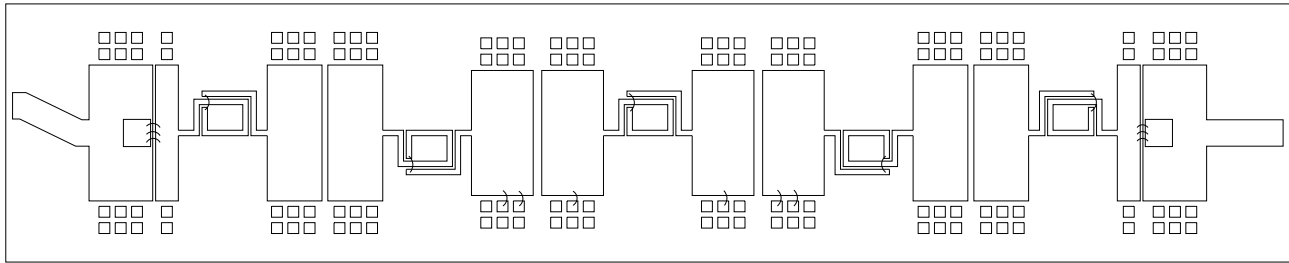
Pseudo-Lumped 3.72 GHz Bandpass Filter

This filter is a lower frequency version of the previous example. The two key parameters for this design were insertion loss and the width of the spurious free stopband. Printed spiral inductors were used to achieve the higher inductance values needed at this frequency.

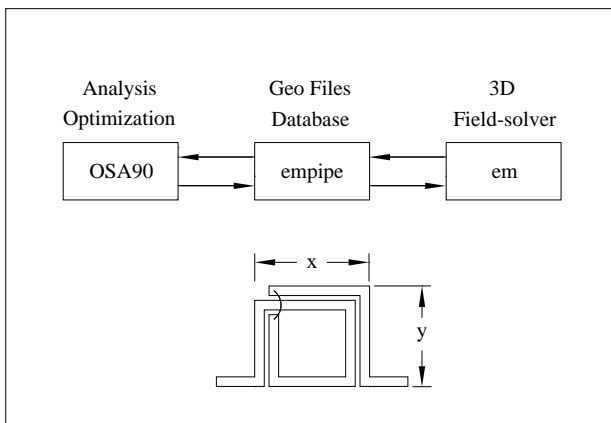
This example demonstrates how the field-solver can now be used to optimize planar circuits. The filter was subdivided into three unique pi-network elements and one spiral inductor element. The analysis and optimization of these "circuit elements" were controlled by a linear simulator, *OSA90*, with

an auxiliary interface to the field-solver, *empipe* [24]. The analysis and optimization proceed by first building a data base of field-solver solutions around the starting point and then interpolating in the existing data base or adding new solutions to the data base. One side benefit of this approach is that it frees the user from the fixed grid. That is, solutions can be found with dimensions that do not fall on the analysis grid. More details on direct driven em optimization can be found in [25,26].

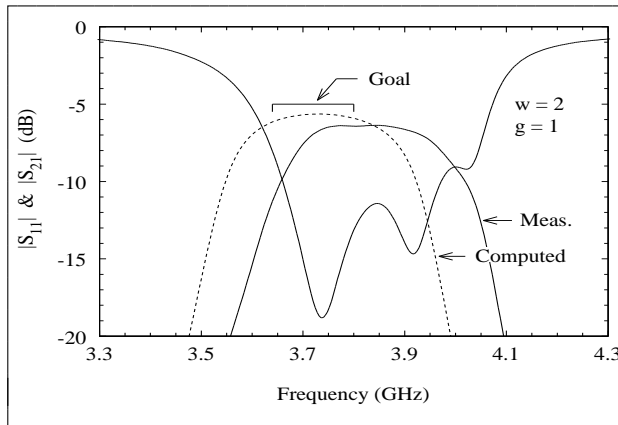
The final layout for this filter is shown below. The substrate is 20 mil thick alumina, 945 mil long by 190 mil wide. A more complete description of this filter can be found in [27].



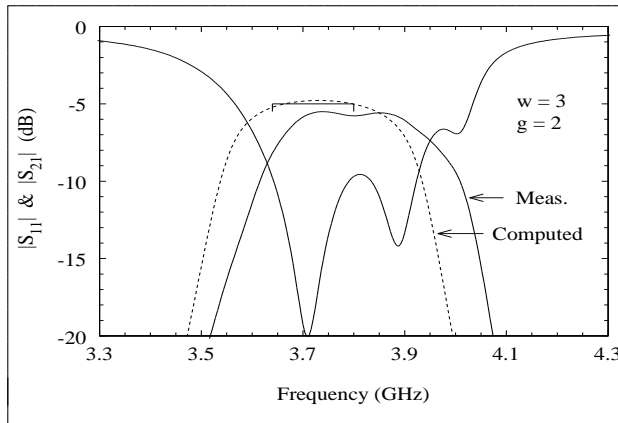
The insertion loss and stopband rejection requirements force a compromise to be made in the spiral inductor design. Wide traces minimize the insertion loss but a narrow trace maximizes the self resonant frequency. In the field-solver modeling there is also a question of convergence. How many cells across the width of the strip are needed to get accurate results? On the left is a subsectioned spiral with 4 mil traces and 2 mil gaps on a 1 mil grid.



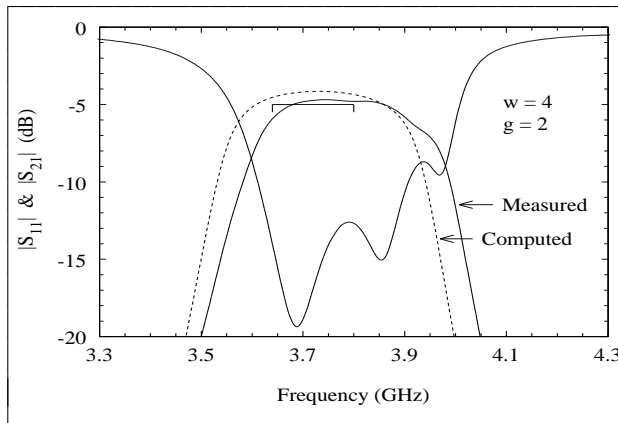
This schematic shows how the linear simulator interfaces to the field-solver. Under the present interface, the spiral inductor and capacitor pi-network are custom circuit elements. Their dimensions are defined in the circuit file and can be optimized just like any other microstrip element. *Empipe* generates new geometry files as needed and interpolates in the data base of results.



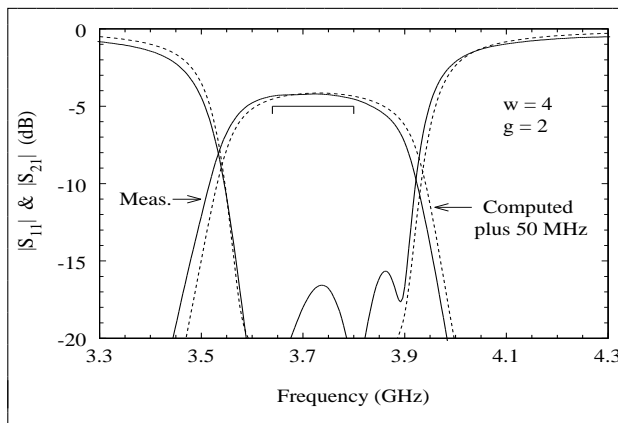
A total of four designs were fabricated and tested for this project. The first design used spiral inductors with 2 mil wide traces and 1 mil gaps. On the left is the turn-on insertion and return loss. The goal for the filter was less than 5 dB insertion loss from 3.64 GHz to 3.80 GHz. The measured inductor Q for this sample is 55 and the center frequency error is 100 MHz or 2.7%.



In the second design the spirals had 3 mil wide traces and 2 mil gaps. Here is the turn-on data for this iteration. The measured inductor Q has increased to 65 and the center frequency error has decreased to 75 MHz or 2%.



The third design had spirals with 4 mil traces and 2 mil gaps. The turn-on data shows an inductor Q very close to 74. The insertion loss has decreased almost 2 dB compared to the first filter and the frequency error is down to 50 MHz or 1.3%. Why did the frequency error decrease? A 1.0 mil grid was used for all the spiral models; the number of subsections across the width increased for each iteration. These three filters were fabricated on the same 2 by 2 inch substrate.



In manufacturing it was desirable to center the turn-on frequency more accurately. To account for the remaining frequency error, the ideal design was shifted 50 MHz low and the optimization was run one more time. The Y-dimension of the spirals changed 0.9 mil in this final optimization. Here are the tuned filter results versus the computer prediction (offset by 50 MHz). Tuning for return loss required 6 pads (8 by 8 mil) to be bonded in. The center frequency error is now about 0.5%.

Conclusion

We started this talk with a very brief introduction to how one field-solver works. Unlike circuit theory based tools, in the field-solver there are many parameters to adjust and a basic understanding of how the tool works is very helpful. Some very basic geometries were used to explore the visualization capabilities of the field-solver. Viewing the current and voltage on these simple test cases leads to insight that can be applied to more complex geometries without actually doing the visualization calculations.

A discontinuity problem can be solved very rapidly on today's field-solvers. One very useful task for the field-solver is validation of existing analytical models. When the validation fails, as is the case of the via hole, new data can be generated to replace an existing model. The microstrip bend computations seem to confirm the analytical model, although a more rigorous validation would include phase data. The field-solver can also generate new models for geometries not found in the standard libraries, the compensated tee-junctions are one example. Optimization can also be applied to compensation problems like the tee-junction. The field-solver user is no longer limited by the imagination of the linear simulator vendor.

Field-solvers can be applied to virtually any microwave component but they are particularly useful for filters. Every small improvement in modeling accuracy contributes to greater accuracy in the final filter design. A hybrid approach that combines the results from several different tools is also a very useful concept. In the microstrip interdigital filter, field-solver models of the via hole and the tee-junction are critical to first pass success. The bandstop filter demonstrated how whole regions of a circuit that include several discontinuities in close proximity can be computed. The 22.5 GHz bandpass filter proved that circuit theory modeling sometimes fails to capture the behavior of a very simple geometry. And the 3.72 GHz bandpass filter shows how the field-solver can be used in an optimization loop and the importance of convergence in field-solver solutions.

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