

A Wideband General Purpose PIN Diode Attenuator



Introduction

PIN diode based AGC attenuators are commonly used in many broadband system applications such as: cable or fiberoptic TV, wireless CDMA, etc. A popular attenuator design utilized over the instantaneous frequency range from 10 MHz to beyond 2 GHz is the PI network. The benefit of this design is its broadband constant impedance, wide dynamic range and good compatibility with AGC signals.

The PIN diode is used as a current controlled resistance component in the PI network. PIN diodes are low cost, low distortion elements available in commonly used small size plastic packages. This application note describes the design of a high performance, PIN based 4 diode PI attenuator utilizing Alpha's low cost SMP1307-011 diode in a plastic SOD-323 package. Performance is characterized from 10 MHz–3 GHz.

PI Attenuator Fundamentals

For matched broadband applications, especially those covering low RF frequencies (to 5 MHz) through frequencies greater than 1 GHz, PIN diode designs are commonly employed. The circuit configurations most popular are the TEE, bridged TEE and the PI. All these designs use PIN diodes as current controlled RF resistors whose resistance values are set by a DC control, established by an AGC loop.

Figure 1 shows the basic PI attenuator that uses 3 PIN diodes. It also shows the expressions that determine the resistance values for each PIN diode as a function of attenuation. Figure 2 displays the value of PIN diode resistance for a 50 Ω PI attenuator. Note that the minimum value for the shunt diodes, R_1 and R_2 , is 50 Ω .

This application note describes the design and performance of a PI attenuator that uses 4 PIN diodes as shown in Figure 3. The benefit of the 4 diode circuit is its symmetry that allows for a simpler bias network and a reduction of distortion due to cancellation of harmonic signals in the back to back configuration of the series diodes.

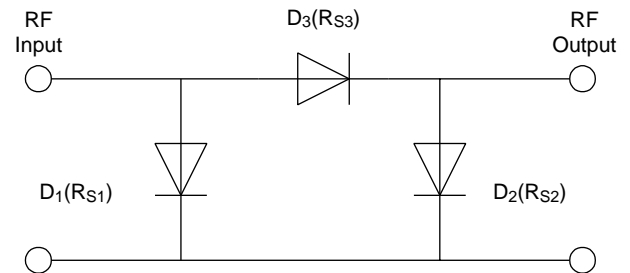


Figure 1. PI Attenuator

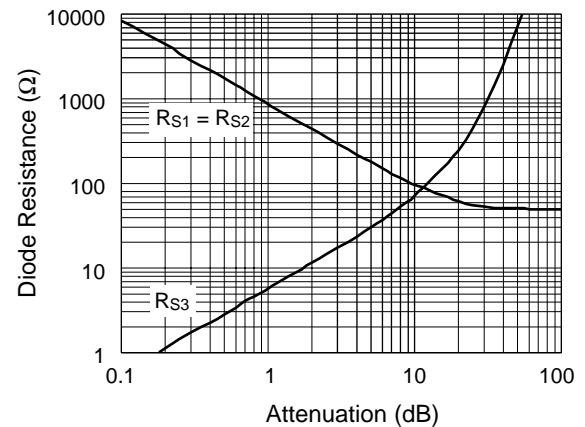


Figure 2. Attenuation of PI Attenuators

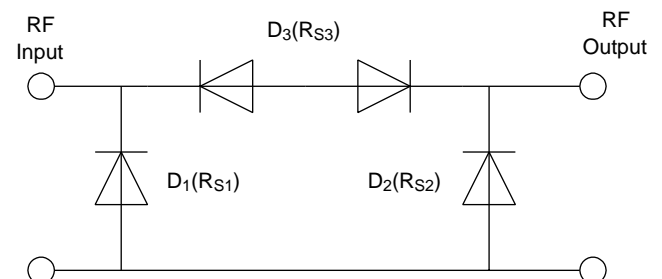


Figure 3. 4 Diode PI Attenuator

Attenuator Circuit Model

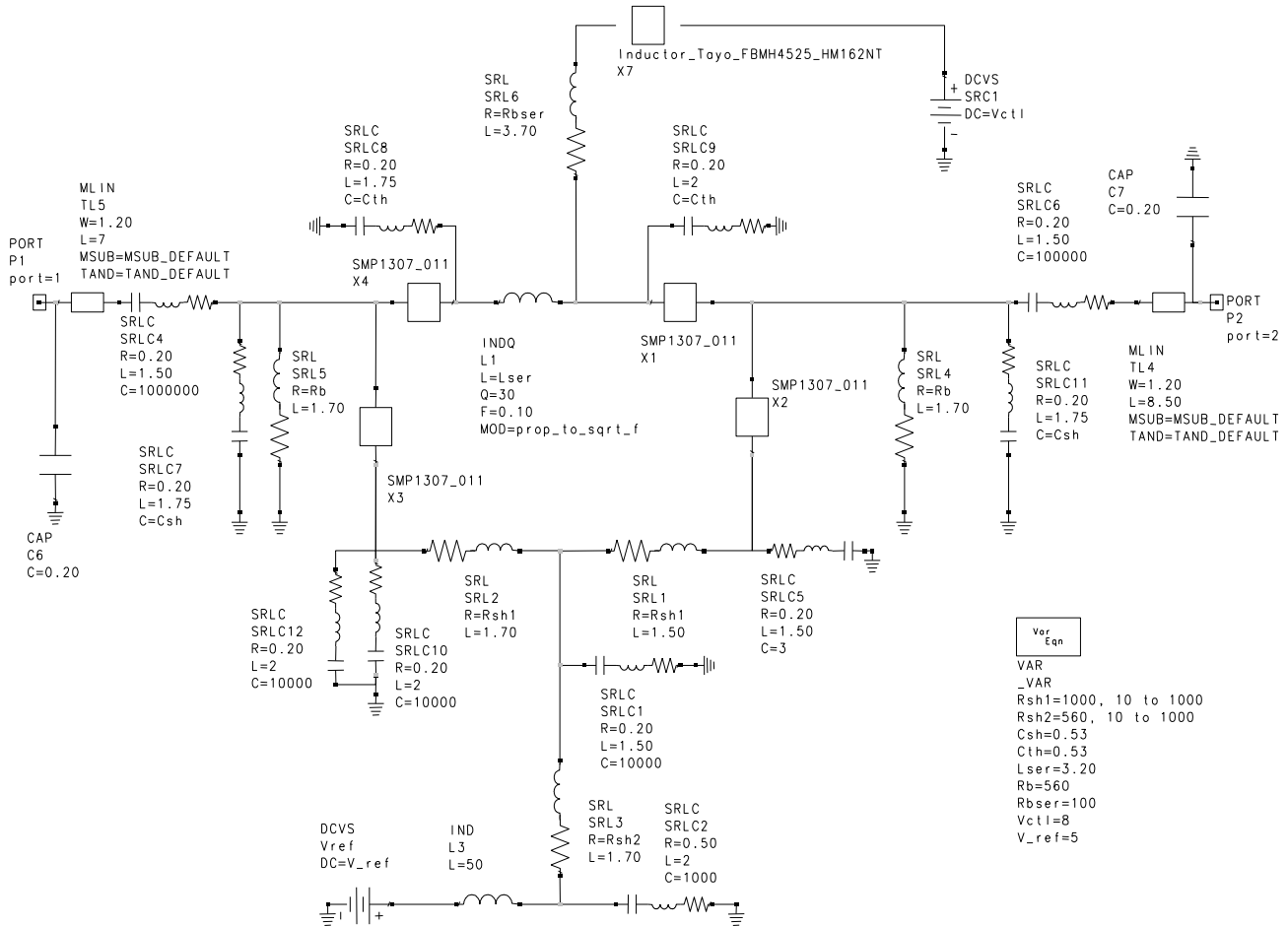
In the Libra IV model shown in Figure 4, the PIN diode pairs, X_3/X_4 and X_1/X_2 , are symmetrically biased from two DC sources. A 5 V reference DC voltage source (V_{REF}) provides adequate biasing to keep the RF resistance of the shunt diodes X_2 and X_3 near $50\ \Omega$ at high attenuation while the series diodes, X_4 and X_1 , are at high resistance values. The values of biasing resistors SRL_3 , SRL_2 , SRL_1 , SRL_5 and SRL_4 were selected to provide low SWR for the full attenuation range. Attenuation is controlled by the control voltage source (V_{CTL}), ranging from 1–6 V. This source supplies forward bias current to the series diodes, X_4 and X_1 , through a wideband, high impedance ferrite inductor, X_7 (Taiyoyuden model FBMH4525) and resistors SRL_5 , SRL_4 and SRL_6 .

Capacitors $SRLC_{12}$, $SRLC_{10}$ and $SRLC_5$ provide RF ground for the shunt diodes. The separation of the biasing path onto two branches SRL_2 and SRL_1 was to reduce RF coupling between input and output, which will affect maximum attenuation especially at high frequencies, due to the parasitic series inductances.

Capacitors C_6 and C_7 simulate the effect of the coaxial connectors (on our test boards we used SMA connectors). Shunt connected capacitors, $SRLC_7$ and $SRLC_{11}$, were inserted to compensate the parasitic inductances of the decoupling capacitors, $SRLC_4$ and $SRLC_6$. These parasitic inductances strongly affect attenuator performance at frequencies beyond 2 GHz.

The PI type C-L-C circuit between series diodes $SRLC_8$, L_1 and $SRLC_9$, was used to increase the maximum isolation at higher frequencies while improving insertion loss at low attenuation. Figure 5 illustrates the effect of connecting or not connecting this C-L-C circuit. A clear 5–8 dB improvement in isolation is demonstrated.

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Var Eqn
 VAR
 _VAR
 Rsh1=1000, 10 to 1000
 Rsh2=560, 10 to 1000
 Csh=0.53
 Cth=0.53
 Lser=3.20
 Rb=560
 Rbser=100
 Vctl=8
 V_ref=5

DATA

TEMP
 TEMP_DEFAULT
 TEMP=27

Var Eqn

UNITS
 UNITS_DEFAULT
 FREQ=GHz
 RES=Ohm
 COND=S
 IND=nH
 CAP=pF
 LNG=mm
 TIME=psec
 ANG=deg
 POWER=dBm
 VOLT=V
 CUR=mA
 DIST=mi

DATA

RREF
 RREF_DEFAULT
 R=50

Var Eqn

_VAR
 lctl=100
 L_cap=0.50

DATA

SIGMA
 SIGMA_DEFAULT
 SIGM=0

DATA

TAND
 TAND_DEFAULT
 TAND=0.10

DATA

MSUB
 MSUB_DEFAULT
 ER=4.20
 H=0.80
 T=5.00e-003
 RHO=0.75
 RGH=0
 COND1=cond
 COND2=cond2
 DIEL1=diel

DIEL2=diel2
 HOLE=hole
 RES=resi

DATA

MSUB
 MSUB_HP
 ER=4.20
 H=0.78
 T=5.00e-003
 RHO=0.75
 RGH=0
 COND1=cond
 COND2=cond2
 DIEL1=diel

DIEL2=diel2
 HOLE=hole
 RES=resi

Figure 4. Attenuator Model for Libra IV

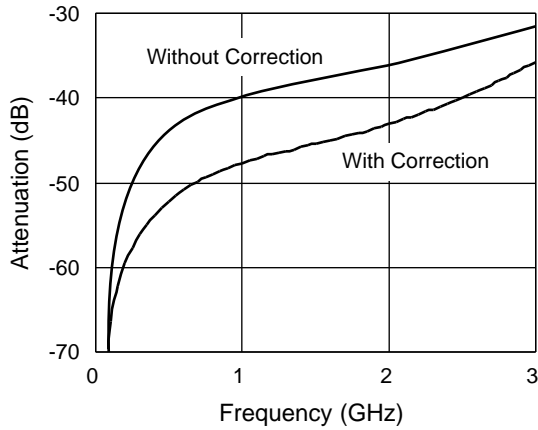


Figure 5. The Effect of Compensation Circuit

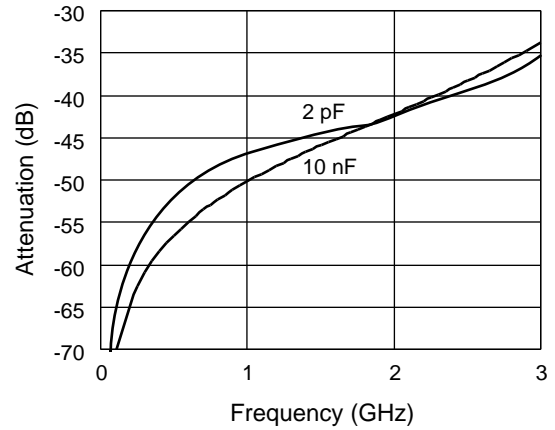


Figure 6. The Effect of Capacitor SRLC₅

The values of the bias resistors were optimized for optimum SWR performance over the entire attenuation range. The intent was to keep the values of SRL₅ and SRL₄ as low as possible to ensure maximum forward current in the series diodes, X₄ and X₁, but high enough not to affect insertion loss.

The input and output circuits are not symmetrical as may be seen from the values of capacitors SRLC₁₂ and SRLC₁₀ (10 nF each), compared to SRLC₅ (2 pF). The SRLC₅ value was selected to improve high frequency isolation by compensating the parasitic series inductance of shunt diode, X₂, and its own parasitic inductance. This compensation was found helpful in improving isolation by several dB at frequencies higher than 1 GHz; however, as a result, the SWR of the output port SWR is increased at lower frequencies.

Most applications are not sensitive to high output SWR, but if necessary, symmetry of the attenuator may be established by increasing SRLC₅ to 10 nF. Figure 6 shows the effect of changing SRLC₅ from 2 pF to 10 nF. If implemented, there will be no significant effect on the input SWR, because of the high isolation between input and output, and no effect on attenuation or SWR at the minimum attenuation.

The linear test bench used for the analysis of the above attenuator is shown in Figure 7.

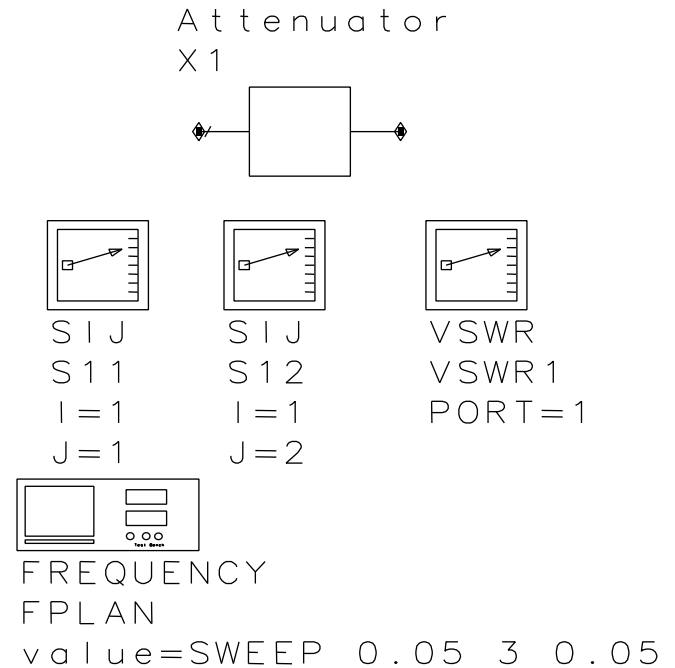


Figure 7. Attenuator Model Test Bench for Libra IV

SMP1307 SPICE Model

The SMP1307-011 is a silicon PIN diode with a thick I-region (175 μm) and a long carrier lifetime (TL = 1.5 μs). This results in a variable resistance device with a wide variation of resistance vs. current capable of operating with low distortion as an attenuator element. The diode is packaged in a SOD-323.

The SPICE model for the SMP1307-011 varactor diode defined for the Libra IV environment, is shown in Figure 8 with a description of the parameters employed. In this model, two diodes were used to fit both DC and RF properties of PIN diode. The PIN diode built-in model of Libra IV was used to model behavior of RF resistance vs. DC current, while PN-junction diode model was used to model DC voltage-current response. Both diodes were connected in series to insure the same current flow, while PN-junction diode was effectively RF short-circuited with the capacitor C₂ = 10¹¹ pF. The portion of the RF resistance, which reflects residual series resistance, was modeled with R₂ = 2.2 Ω. This is shunted with the ideal inductor L₁ = 10¹⁹ nH to avoid affecting DC performance. Capacitances C_G, C_P and inductor L₂ reflect junction and package properties of SMP1307-011 diode.

The described model is a linear model that emulates the DC and RF properties of the PIN diode when the signal frequency is higher then:

$$\frac{1300}{W [\mu\text{m}]^2} = \frac{1300}{175^2} = 0.0425 \text{ MHz}$$

For more details on the properties of the PIN diode refer to Reference 1.

Tables 1 and 2 describe the model parameters. They show default values appropriate for silicon varactor diodes that may be used by the Libra IV simulator. Some of the values of PIN diode built-in model of Libra IV were not used. Those are marked "Not used" in the tables.

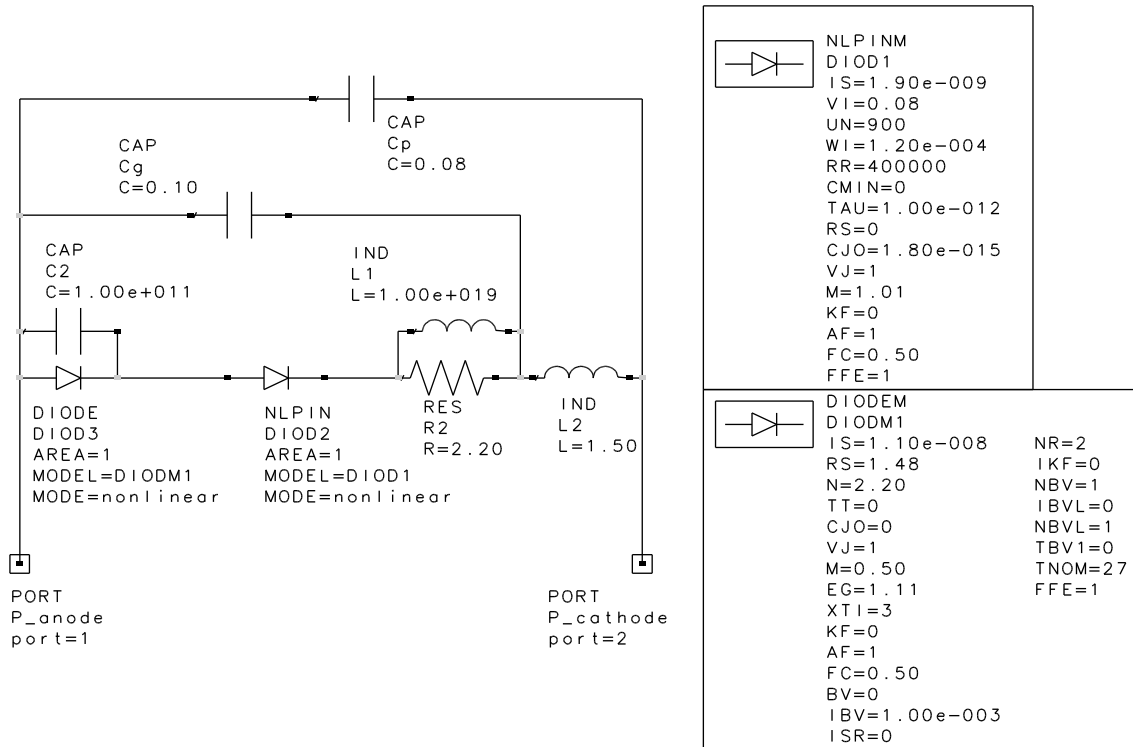


Figure 8. SMP1307-011 Model for Libra IV

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Parameter	Description	Unit	Default
IS	Saturation current (Not used)	A	1.9E-9
V _I	I-region Forward Bias Voltage Drop	V	0.08
UN	Electron Mobility cm ² /(V*S) (Not used)	cm ² /(V*S)	900
WI	I-region Width (Not used)	M	1.2e-4
R _R	I-region reverse bias resistance	Ω	4E5
C _{MIN}	PIN punchthrough capacitance	F	0
TAU	Ambipolar lifetime within I region (Not used)	S	1E-12
R _S	Ohmic resistance	Ω	0
C _{JO}	Zero-bias junction capacitance	F	1.8E-15
V _J	Junction potential	V	1
M	Grading coefficient	-	1.01
KF	Flicker-noise coefficient (Not used)	-	0
AF	Flicker-noise exponent (Not used)	-	1
FC	Coefficient for forward-bias depletion capacitance (Not used)	-	0.5
FFE	Flicker noise frequency exponent (Not used)	-	1

Table 1. Silicon PIN Diode Values in Libra IV Assumed for SMP1307 Model

Parameter	Description	Unit	Default
IS	Saturation current	A	1.1E-8
R _S	Series resistance	Ω	1.48
N	Emission coefficient (Not used)	-	2.2
TT	Transit time (Not used)	S	0
C _{JO}	Zero-bias junction capacitance (Not used)	F	0
V _J	Junction potential (Not used)	V	1
M	Grading coefficient (Not used)	-	0.5
E _G	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E _G , helps define the dependence of IS on temperature)	-	3
KF	Flicker noise coefficient (Not used)	-	0
AF	Flicker noise exponent (Not used)	-	1
F _C	Forward-bias depletion capacitance coefficient (Not used)	-	0.5
B _V	Reverse breakdown voltage (Not used)	V	Infinity
I _{BV}	Current at reverse breakdown voltage (Not used)	A	1e-3
ISR	Recombination current parameter (Not used)	A	0
NR	Emission coefficient for ISR (Not used)	-	0
IKF	High-injection knee current (Not used)	A	Infinity
NBV	Reverse breakdown ideality factor (Not used)	-	1
IBVL	Low-level reverse breakdown knee current (Not used)	A	0
NBVL	Low-level reverse breakdown ideality factor (Not used)	-	1
T _{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker noise frequency exponent (Not used)	-	1

Table 2. Silicon PIN Diode Values in Libra IV Assumed for SMP1307 Model

The model DC current voltage response calculated by Libra IV is shown in Figure 9A together with the measured data. It shows very good compliance of our model DC properties with measured results.

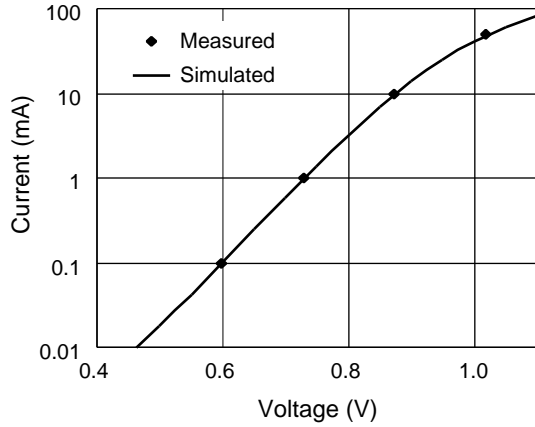


Figure 9A. DC Voltage Current Response of SMP1307-011

Figure 9B shows internal RF resistance after the parasitic capacitances C_G , C_P and inductor L_2 were deembedded. Here again, the measured and simulated results are in agreement.

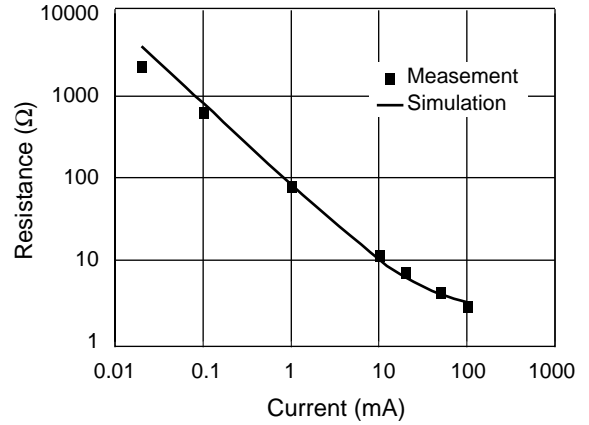


Figure 9B. RF Resistance vs. Current for SMP1307-011

Attenuator Design, Materials, Layout and Performance

The circuit diagram for the 4 diode PI attenuator is shown in Figure 10.

The PCB layout is shown in Figure 11. The board was made of standard, 30 mil thick, FR4 material.

The bill of materials used is shown in Table 3.

Designator	Value	Part Number	Footprint	Manufacturer
C1	10,000 p	0603AU103JAT9	0603	AVX
C2	0.5 p	0603AU0R5JAT9	0603	AVX
C3	10,000 p	0603AU103JAT9	0603	AVX
C4	10,000 p	0603AU103JAT9	0603	AVX
C5	10,000 p	0603AU103JAT9	0603	AVX
C6	10,000 p	0603AU103JAT9	0603	AVX
C7	2 p	0603AU2R0JAT9	0603	AVX
C8	0.5 p	0603AU0R5JAT9	0603	AVX
C9	0.5 p	0603AU0R5JAT9	0603	AVX
C10	0.5 p	0603AU0R5JAT9	0603	AVX
C11	10,000 p	0603AU103JAT9	0603	AVX
C12	10,000 p	0603AU103JAT9	0603	AVX
D1	SMP1307-011	SMP1307-011	SOD-323	ALPHA IND.
D2	SMP1307-011	SMP1307-011	SOD-323	ALPHA IND.
D3	SMP1307-011	SMP1307-011	SOD-323	ALPHA IND.
D4	SMP1307-011	SMP1307-011	SOD-323	ALPHA IND.
L1	1x8 mm	MSL	1x8 mm	(Printed on PCB)
L2	1x8 mm	MSL	1x8 mm	(Printed on PCB)
L3	2.2 nH	LL1608-F2N2S	0603	TOKO
L4	FBMH4525	FBMH4525_HM162NT	1810	TAIYO-YUDEN
R1	560	CR10-561J-T	0603	AVX
R2	100	CR10-101J-T	0603	AVX
R3	1 k	CR10-102J-T	0603	AVX
R4	1 k	CR10-102J-T	0603	AVX
R5	1 k	CR10-102J-T	0603	AVX
R6	560	CR10-561J-T	0603	AVX

Table 3. The Attenuator Bill of Materials

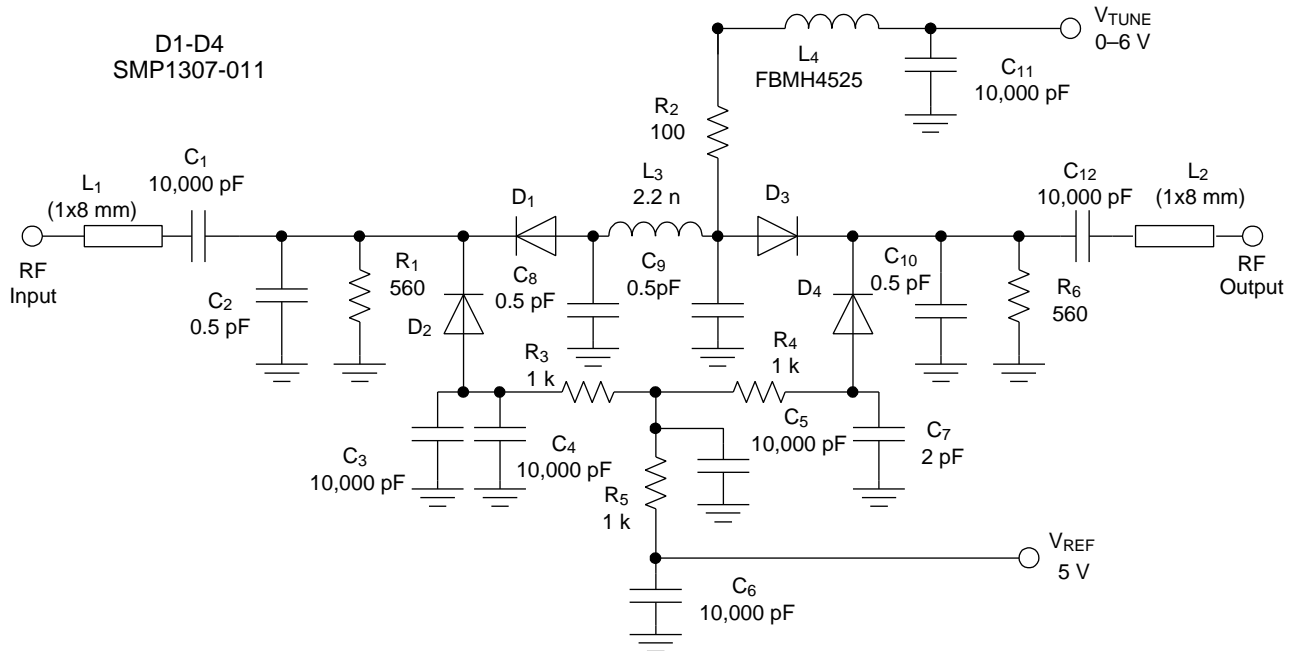


Figure 10. Attenuator Circuit Diagram

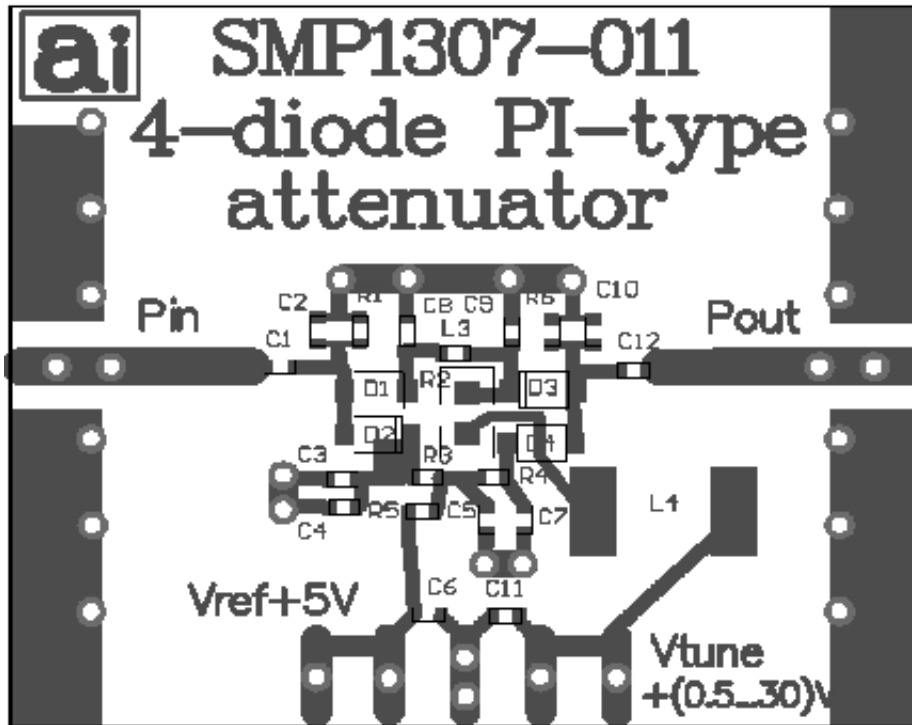


Figure 11. Attenuator PCB Layout

The measured attenuation of this circuit and the simulated results obtained with the model in Figure 8 are shown in Figure 12A and 12B respectively. The model fits measurement results very well in the attenuation extremes, but has a small deviation from measurements in the middle of the attenuation range. This may be attributed to the imperfection of diode RF resistance model shown in Figure 9B.

Figure 13 shows measured input SWR at different control voltages. SWR is well below 2 across the entire range of frequencies and attenuation levels as predicted by the model.

A plot of attenuation vs. control voltage at temperatures of 23°C and 85°C temperatures are shown in Figure 15. The graph shows that the temperature performance is very stable, with less than 0.5 dB variation over the 62°C excursion at the highest attenuation.

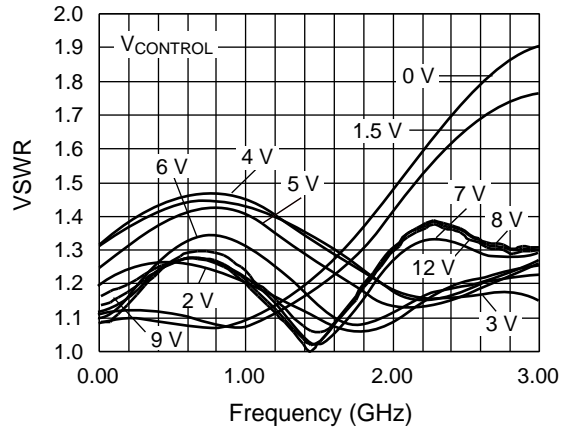


Figure 13. Measured SWR

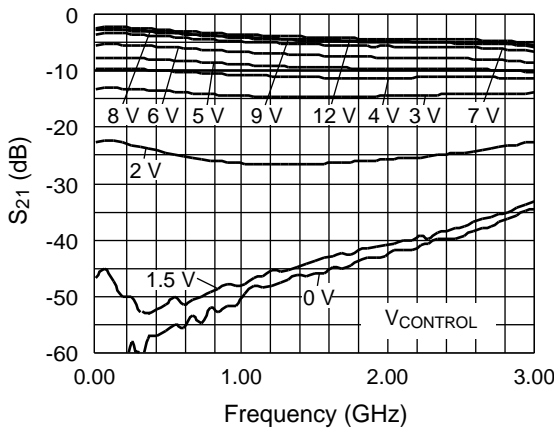


Figure 12A. Measured S_{21}

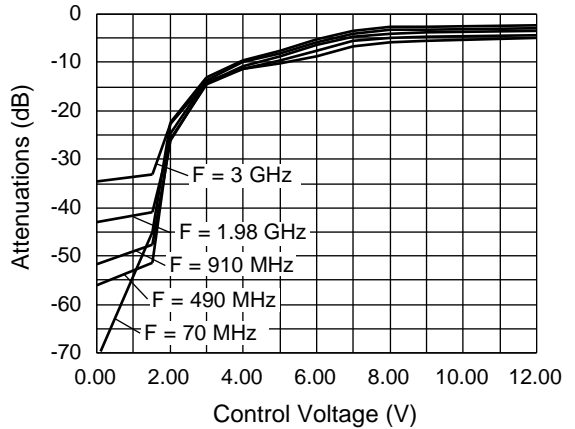


Figure 14. Attenuation vs. Control Voltage

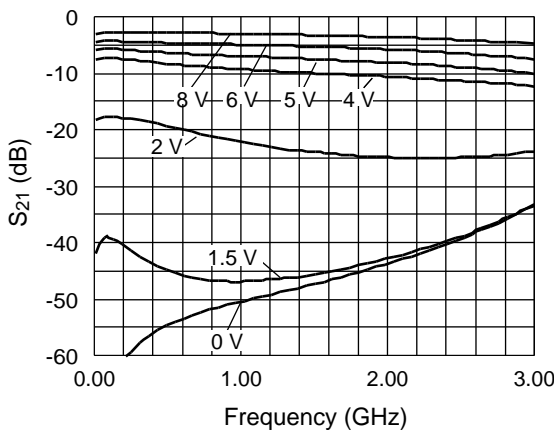


Figure 12B. Simulated S_{21}

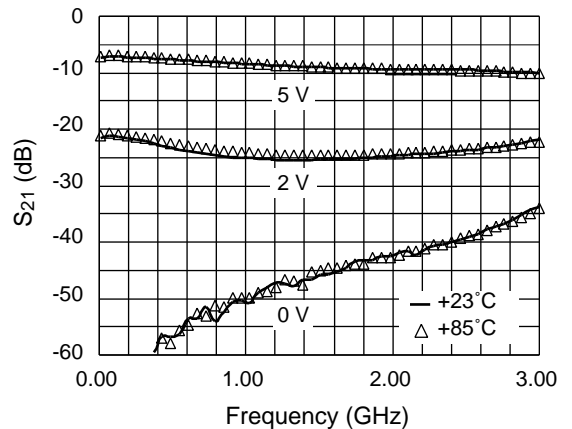


Figure 15. Attenuation vs. Temperature

Figure 16 shows output third order intercept point (IP3) vs. control voltage. The measurement was performed at 900 MHz using a single tone 1 W input power. IP3 was derived from the third harmonic using the method described in Reference 2.

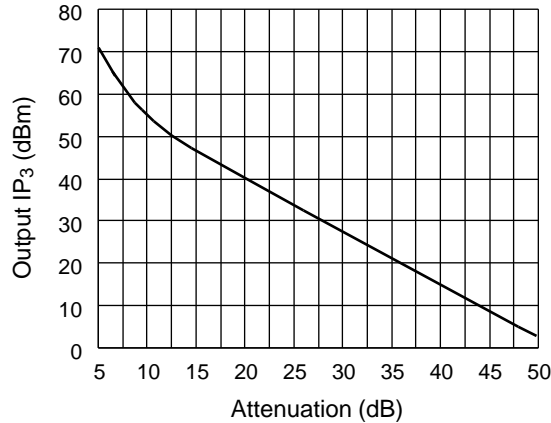


Figure 16. Third Order Intercept Point vs. Attenuation at 900 MHz

References

1. Gerald Hiller, "Design with PIN Diodes," Application Note, Alpha Industries Inc.
2. Gerald Hiller, "Predict Intercept Points in PIN-Diode Switches," *Microwaves & RF*, Dec. 1985.
3. Robert Caverly and Gerald Hiller, "Distortion in PIN Diode Control Circuits," *IEEE Trans. Microwave Theory Tech.*, May 1987.

List of Available Documents

1. The 4-diode PIN attenuator simulation project files for Libra IV.
2. The 4-diode PIN attenuator circuit schematic and PCB layout for Protel EDA Client 1998 version.
3. The 4-diode PIN attenuator PCB Gerber photo-plot files.

Author Information

Gerald Hiller is Senior Scientist at Alpha Industries specializing in control circuit designs using PIN diodes. He has authored more than 20 papers on the subject of PIN diode applications in RF and microwave circuits. Of particular importance is the distortion model for PIN diodes, the impedance vs. frequency characteristic and the reverse bias requirement in high power switches.

Gerald Hiller joined Alpha Industries as Applications Engineering Manager in 1995. In prior years he held similar positions at MA-COM Inc. and Unitrode Corp. Mr. Hiller received the BEE degree at the City College of New York and MSEE degree from the University of Pennsylvania.

Peter Shveshkeyev received his MS and PhD degrees in technical science and engineering from Moscow Technical University of Communications and Informatics in 1981 and 1989, respectively. Since 1981, he has worked on MESFET large-signal device design, developing both software and practical devices. In 1995 he joined Computer and Communications Laboratories of ITRI in Taiwan, developing VCOs for wireless projects. He has been with Alpha Industries as an applications engineer since 1998.

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